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FPGA Implementation of ECG Signal Processing for Use in a Neonatal Heart Rate Monitoring System †

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Abstract: An FPGA based hardware accelerator for bio-signal digital filtering in a neonatal heart rate monitoring system employing electric potential sensors (EPS) is presented. The proposed system contains a single hardware filter stage for antialiasing, with the remaining digital signal processing required to provide a clinical standard ECG performed on an FPGA (National Instruments myRIO 1900). This is compared with a previous microprocessor version (Raspberry Pi 3, BCM2837 processor) containing a dual hardware/software filtering scheme, with the aim of simplifying the analog front end and allowing for reconfigurable filtering in the digital domain. A custom neonate phantom was employed to emulate real world conditions and ambient noise. The developed FPGA system was shown to have a signal quality comparable with the microprocessor implementation, with an average signal to noise ratio loss of 2%. A 12 dB increase in attenuation of the predominant 50 Hz noise and a 90% reduction in energy per sample filtered was shown compared to the microprocessor version, indicating both efficiency and filter effectiveness gains. The phantom was used to broadcast data from the preterm infant cardio-respiratory signals database (PICSDB) and the FPGA filtering scheme was shown to remove the majority of the ambient 50 Hz noise with an average reduction of 30 dB, and provided a clean ECG signal. These results demonstrate that FPGA filtered EPS ECGs have comparable signal quality to the combined HW/SW filtering implementation, with a reduction in complexity and power consumption.

Keywords: heart rate; FPGA; ECG; newborn; medical devices; DSP; electric potential sensor

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1. Introduction

The need for rapid and accurate heart rate (HR) measurement in the delivery room is well established, as it is the predominant quantitative indicator of a newborn's health and is monitored in the delivery room to guide clinical intervention and resuscitation efforts [1]. Our previous work describes a prototype microprocessor based neonatal HR monitor [2] integrating novel electric potential sensors (EPS) into a standard delivery room neonatal mattress. EPS sensors do not require galvanic contact with the skin, therefor high resolution ECGs can be recorded without the need for sensor attachment allowing for rapid and accurate infant HR calculation. EPS sensors are highly susceptible to ambient noise however, predominantly 50/60 Hz power line interference. The requirement for high levels of filtering with EPS devices can be fulfilled by the use of hardware accelerators in place of traditional digital signal processing.

Field programmable gate-arrays (FPGAs) are reprogrammable logic devices, capable of parallel process execution and reconfiguration. FPGA based bio-signal filtering has been successfully applied to the ECG signal for powerline noise reduction [3] with efficiency savings over traditional DSP, and FPGA implementations of beat detection

algorithms used to measure heart rates. have shown a 98% accuracy and real-time beat classification [4].

FPGA system on chip (FPSoC) architectures provide dynamic partial reconfiguration (DPS) for runtime reconfiguration of the FPGA [5] which can replace static analog front-end elements such as analog hardware filters. This allows for adaptation to changing or intermittent noise sources.

This work considers the implementation of an FPGA based digital filtering system for electrocardiogram reading using EPS sensors. Two platforms are tested: a microprocessor-based system with both hardware and software filters; and an FPGA based system with a single hardware low pass filter stage for anti-aliasing, and software filtering. Both systems are characterized using a custom infant ECG phantom tailored for EPS sensor experimentation. Evaluation metrics for signal quality were defined including signal quality, noise rejection and HR calculation accuracy. The end goal being to investigate whether the hardware filtering section can be removed and replaced with a purely digital filtering scheme implemented in FPGA hardware.

2. Materials and Methods

This work compares two neonatal HR monitoring platforms, being the frontend for the EPS sensors: a traditional microprocessor based system and a field programmable gate array based system, hereafter referred to as the μPU and FPGA systems respectively. Both systems are connected to a pair of EPS sensors, with a textile reference electrode connected to each system ground. A subtraction is performed by a precision instrumentation amplifier (AD623) to remove common mode noise and produce a single signal which is processed by the system front ends. Figure 1 shows a block system diagram of the EPS sensor connections to the frontend and system architecture elements.

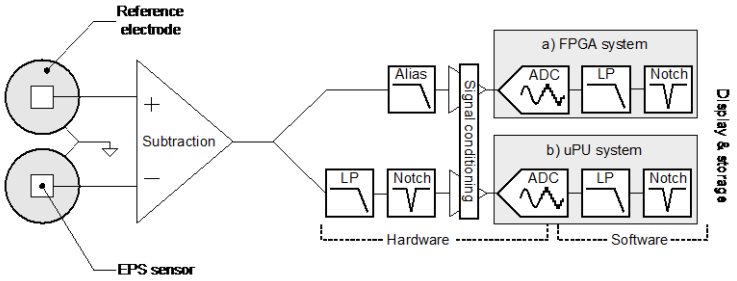

Figure 1. EPS sensor connection & system architecture overviews. a) FPGA system, b) μPU system.

The μPU system is based on the Raspberry Pi 3 A+ with built-in hardware filtering, a 12 bit analog to digital converter (ADC) sampling at 1 kHz. A C++ DSP filtering runs on Raspbian Linux using the Broadcom 2837 (Cortex-A53). The resulting data is displayed on an integrated 7″ touchscreen and graphical user interface. The FPGA system is based on a National Instruments myRIO 1900 platform with a front end for signal conditioning and alias filtering. A 12 bit ADC at a sample rate of 1 kHz matches that of the μPU system. Digital software filters are implemented in the FPGA portion of the Xilinx Z-7010 chip. Data storage and display is programmed in National Instruments LabVIEW.

2.1. Filtering

A 50 Hz notch filter to remove the dominant noise from powerline interference, and a 200 Hz low pass (LP) filter to remove any higher frequencies and harmonics of the fundamental 50 Hz noise are employed. These standard ECG filter specifications are chosen to avoid any alteration of the ECG signal [6], and allow the R peak of the ECG to be extracted accurately, enabling heartbeat interval and therefore HR calculation. Figure 2 shows the frequency response of the hardware and software filter stages.

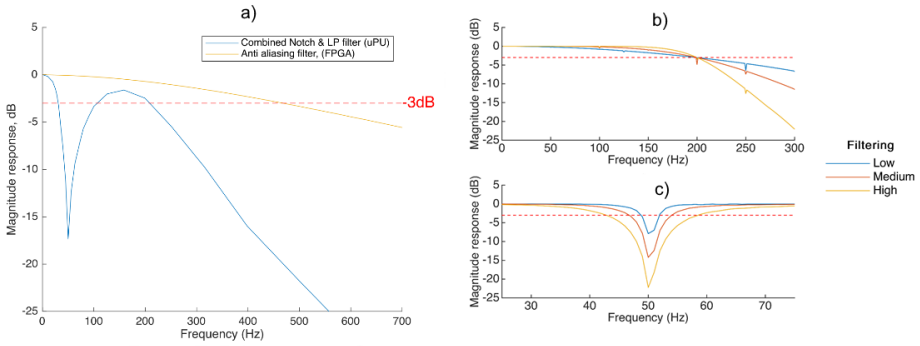

Figure 2. (**a**) Hardware, (**b**) software low pass and (**c**) software notch filter FRA.

Hardware filtering for the μPU system consists of a 2nd order active twin-T Notch filter (corner frequency, fc = 50 Hz) and a 2nd order active low pass filter (fc = 200 Hz) and the FPGA system contains a single 1st order active low pass filter (fc = 500 Hz) for anti-aliasing, as shown in Figure 2a.

Both systems have the same software filters implemented in the FPGA or C++ respectively. To compare different levels of software filtering 3 predefined filtering settings were defined as Low/Medium/High. The level of high frequency (>200 Hz) attenuation for the LP filters is controlled by varying the filter order, thus creating a steeper rolloff as seen in Figure 2b. The level of 50 Hz attenuation is varied by varying the stopband frequencies either side of 50 Hz resulting in a deeper notch (Figure 2c).

2.2. Neonate Phantom

A cardiac phantom was developed to mimic the interference layer of tissue between signal source and sensor, and to provide a signal ground path with similar conductivity to human tissue. It consists of a stack of layers modelling the voltage of the neonate heart and signal propagation through the human tissue, the cotton & foam material of the mattress.

Pharmaceutical-grade agar powder (Intralabs UK) used at 2% concentration (to reflect the elastic behaviour of skin) was mixed with a saline solution to increase the conductivity. 1 mg NaCl per 100 mL was selected for an approximate conductivity of ≈0.5 Siemens/m to emulate the skin as described in [7]. Agar castings were then placed on top of an insulating base with a copper ground loop and voltage source emitter for signal generation.

The EPS sensors and ground reference electrodes (CuNi MOS Titan conductive fabric) are attached to a cotton substrate to mimic the top layer of a delivery room mattress. Electrodes were selected for biocompatibility, low electrical resistance and an impedance comparable with traditional ECG electrodes [8] of 100 kΩ at 50 Hz. To reproduce the compression due to an average birth weight infant (~3.4 kg), a weight of 140 g was placed on top of the phantom stack to achieve a realistic contact pressure of 260 Pa for the 5 cm × 10 cm stack.

2.2. Signal Analysis

SNR was calculated using the signal matching method [9]. A 2 Hz sine wave with amplitudes of Vpp = 25 mV, 50 mV and 75 mV was transmitted to the phantom. EPS sensor voltages drop linearly with distance from the source, representing EPS voltages of 3.3, 6.7 and 10 mV respectively, comparable to infant ECG voltage levels. Five 60 s recordings of the test signal were taken with both systems, then an idealised input sine wave was then generated, and cross correlated with the recorded signal in MatLab. This was used to produce a noise estimate by subtracting the idealised sine wave from the recorded EPS output. The signal-to-noise ratio (SNR) in decibels of the signal is then derived by computing the ratio of its summed squared magnitude to that of the noise.

The phantom was used to transmit a generated neonate biosignal to the EPS sensors at an amplitude of 75 mVpp at 1, 2 and 3 Hz corresponding to 60, 120 and 180 bpm. This serves to examine the frequency components of the received signal, and to examine the calculated HR and any system induced heart rate variability. The Pan Tompkins HR detection algorithm [10] was applied to validate accurate HR calculation, and the heart rate variation (HRV) metric rrHRV [11] (computing the difference of consecutive RR intervals weighted by their mean) was also applied to the signals.

Finally, to test filtering effectiveness of the proposed FPGA system with real world signals the neonate phantom was used to broadcast 60 s samples of waveforms from the Preterm Infant Cardio-Respiratory Signals Database [12].

Data was recorded and processed in MatLab, and recordings were made simultaneously on both devices in a residential setting with no attempt to shield the devices from ambient interference that may be present.

3. Results

Figure 3 shows the results comparing the SNR of the DSP filtering of the FPGA system to the combined DSP & hardware filtering of the µPU at a range of signal amplitudes:

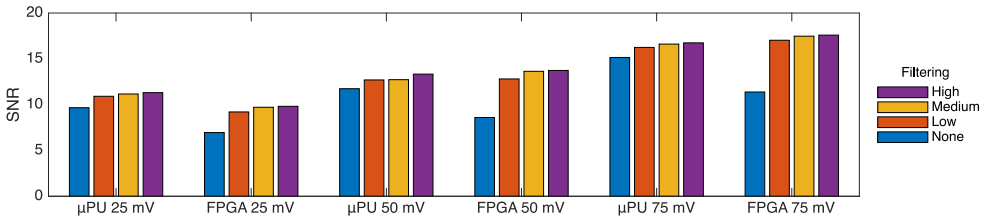

Figure 3. Signal to noise ratio for both systems at a range of signal amplitude and DSP filtering levels.

SNR is proportional to the signal amplitude as the predominant 50 Hz noise (external to the system) is fixed, so increasing signal amplitude increases the SNR. For the High filtering case (ideal scenario) the FPGA has a 15% reduction in SNR compared to the µPU system at the 25 mV signal level, but a 3% and 5% increase for the 50 mV and 75 mV signal levels respectively. This gives the FPGA system an average SNR loss of 2% compared to the µPU system, indicating that the signal quality is comparable. The effect of increasing the level of filtering is modest, and for all the cases across both devices the High filtering level only generates a maximum 7% increase in SNR compared to the Low level. Comparing the unfiltered µPU cases, the effect of the hardware filtering stage is clear accounting an average increase of 3 dB SNR compared to the unfiltered FPGA system.

Figure 4 shows the PSD using the Welch estimate method for a generated neonate biosignal transmitted to the phantom with an amplitude of 75 mVpp at 120 Hz.

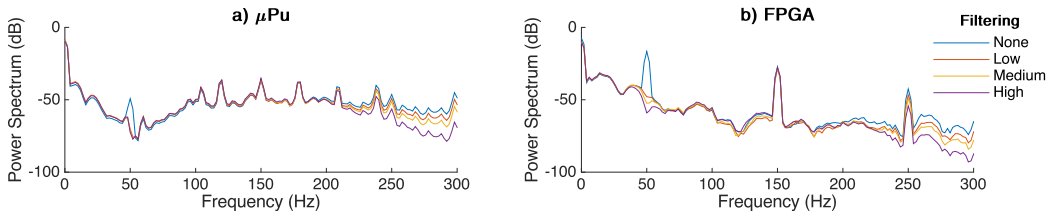

Figure 4. PSD of a generated neonate biosignal for (**a**) µPU system, (**b**) FPGA system.

For both cases, without DSP filtering the 50 Hz noise peak can be seen clearly, although having lower amplitude for the µPU system given that the signal has already been pre-filtered using the hardware filtering. The varied levels of DSP filtering provide greater 50 Hz attenuation for the FPGA system at 29.2, 33.8 and 40.4 dB for low/medium/high respectively, and just 28 dB for the µPU across all 3 DSP filtered cases. The effect of the

increased DSP filtering levels is clear for all the LP filters, with increasing rolloff visible for both systems above 200 Hz, closely matching the frequency response analysis in Figure 2b&c. The results of the HR validation and HR variation analysis are presented in Table 1, to quantify the temporal accuracy of both systems.

Table 1. HR and HRV analysis at a range of heart rates.

	μPU			FPGA		
Generated HR, bpm	60	120	180	60	12	180
Calculated HR, bpm	60	120	180	60	12	179
rrHRV, median	0.22	0.62	0.81	0.14	0.28	0.42

In this test, the two systems produced HRs within 1 bpm of the generated signals, confirming the accuracy of the signal reproduction. The HRV analysis showed increasing RR interval deviation for increasing bpm due to the fixed 1 kHz sample rate of the devices, where higher frequency input samples become less temporally accurate due to sample timing errors in discretization.

A sample of the results of the PICSDB waveform testing of the FPGA system is shown in Figure 10:

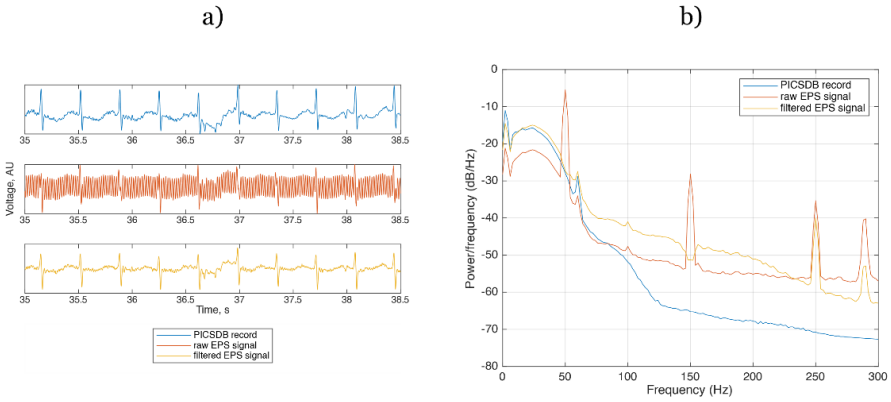

Figure 5. Sample data from PICSDB filtering (record ecg8).

Figure 5a shows the original signal, the effect of the addition of ambient 50 Hz noise in the raw EPS signal, and the filtered EPS signal showing the removal of noise and return to original waveform morphology. The R peak of the ECG is clearly visible in the filtered signal, albeit with some reduction in amplitude. Features of the ECG such the baseline wander just after the 36.5 s mark are preserved in the filtered signal, showing that no major morphological changes occur in the waveform. In Figure 5b the PSD of PICSDB record, raw signal, and filtered signal are shown. The susceptibility of EPS sensors to 50 Hz noise is clear in the peaks at 50 Hz and also 150 Hz harmonic. The FPGA based filtering scheme removed an average of 30 dB of 50 Hz noise via the notch filter, and the steep rolloff of the 200 Hz LP filter removed the higher order harmonics.

4. Discussion

Signal quality for the proposed FPGA DSP system is broadly equivalent to the μPU with hardware & software filtering, with an average SNR loss of just 2%. The frequency response of the FPGA is shown to have up to twice as much 50 Hz noise attenuation for the highest filtering setting compared with the μPU system. Heart rate variability measurements using a HR detection algorithm and analysis of detected RR interval changes show that both systems produce ECGs suitable for the accurate calculation of heart rates (within 1 bpm of the generated signal).

This work has introduced an FPGA based DSP filtering system for the monitoring of newborn ECG signal using electric potential sensors, validating its performance using a neonate phantom with a high resolution, low amplitude bio-signals and a human tissue phantom. The system is characterised and compared to a previous prototype with microprocessor-based software DSP. The FPGA system is shown to have the same filtering capabilities compared to the μPU system, despite the lack of hardware filtering stage, and consuming up to 90% less energy per sample filtered. The FPGA system recorded ECGs suitable for the accurate calculation of HR, and with less HR variation than the μPU system. This work contains strong evidence that sufficient filtering capacity is available purely in the digital domain by harnessing FPGA technology.

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