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# Design and Analysis of a Three-Phase 3L-ANPC Inverter for Electric Traction

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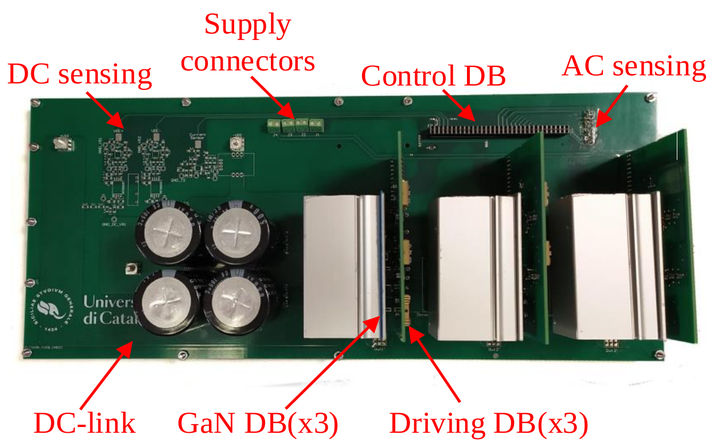
## INTRODUCTION & AIM

Traction electric drives are required to feature high efficiency, compactness, high power density, high reliability and low weight. Though gallium nitride (GaN) technology presents a promising opportunity to achieve this target, their 650V breakdown voltage makes them unsuitable to be exploited in traditional power conversion units with 800V dc-buses. The use of multilevel inverters is thus imperative to combine the exploitation of this technology with increased charging voltages that are currently pursued by manufacturers. Among multilevel converters topologies, Active Neutral Point Clamped (ANPC) offers the best distribution of switching and conduction devices losses.

The core of the presented activity is the design methodology and the analysis of a **800V 11kVA three-phase three-level ANPC**, utilizing 650V GaN enhancement-mode high-electron mobility (HEMT) transistors for electric traction systems.

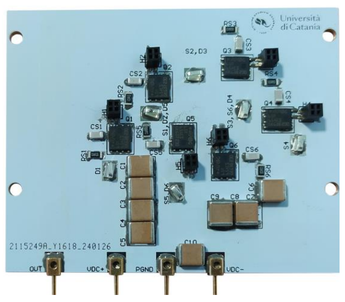
## METHOD



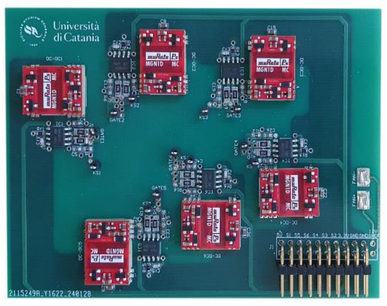

3D top view of the designed main board.

The proposed design consists of four kinds of boards corresponding to the four different sections that make up the **modular power conversion unit**: main board, three GaN daughterboards (DBs), three driving DBs, two alternative control DBs.

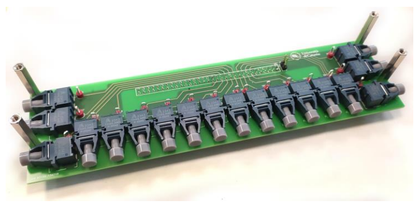
- **Main board's modular design** allows to change topology, GaN packages and stackup technologies just designing new DBs with easier layout, saving time and costs. In addition, modularity allows to sunder power and signal sections, reducing interferences and optimizing the overall size of the power converter.
  - **GaN DB** consists of an ANPC single-phase power cell realized using IMS technology which offers low case-to heatsink thermal resistance to maximize power devices' heat dissipation. It is made up of six SGT65R65AL GaN HEMTs, decoupling capacitors and RC snubbers.
  - **Driving DB** consists of DC/DC stage and driving circuit for GaN HEMTs. The use of dual output 6V/-3V DC/DC converters allows to significantly reduce the length of the conductive paths and the overall size of the driving section. GaN and driving DBs are orthogonally connected to each other. Gate and Kelvin source pins of GaN HEMTs in the GaN DB are connected to the respective gate drivers' outputs and HV isolated grounds in the driving DB.
  - **Control DB** is responsible for providing PWM signals to gate drivers in two alternative versions. Optic DB consists of optical receivers which allow to control GaN HEMTs with FPGA, STM32 NUCLEO or dSpace. STM32 DB consists of a STM32-G474QET6-adapter.



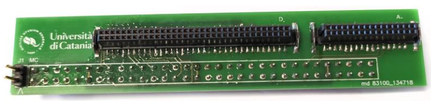
GaN daughterboard.



Driving daughterboard.



Optic control daughterboard.

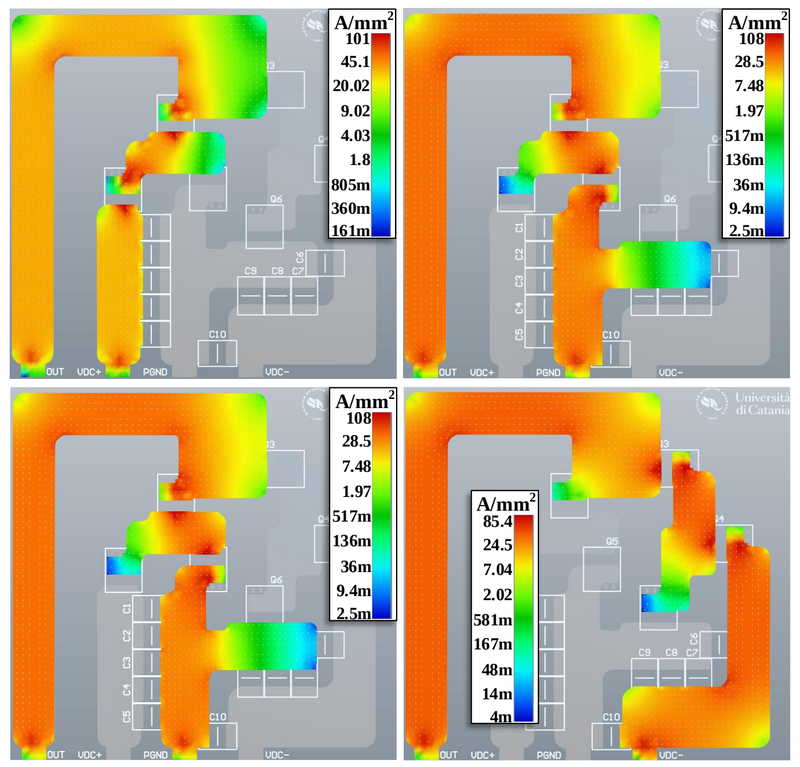


STM32-adapter.

- **Thermal analysis** was conducted in GaN DB to dimension heatsink for GaN HEMTs' cooling and to correctly design power traces avoiding bottlenecks and limiting hot spots on the PCB.
  1. Assuming steady-state conditions and that the 6 devices of each leg are equal heat sources, the required heatsink's thermal resistance can be evaluated as:

$$R_{sa} = \frac{T_j - T_a}{6P_{tot}} - R_{TIM} - R_{IMS} - R_{FR4} - R_{Cu} - \frac{R_{jc}}{6}$$

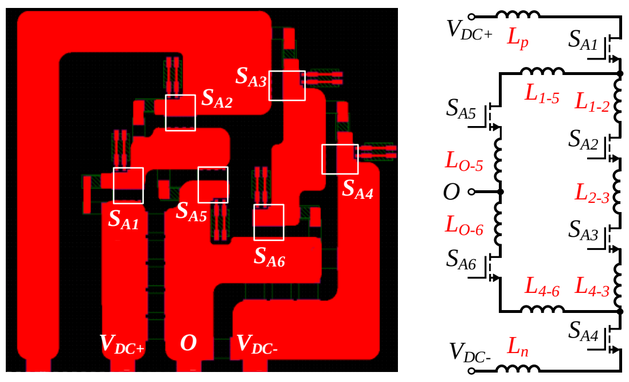
  2. Presence of eventual hot spots was investigated by means of Altium PDN Analyzer. Since the tool allows to work only in dc conditions, simulation was carried out individually considering the four feasible ANPC power cell's states. Dc current density distribution was plotted in heat maps in post-processing.




Dc current density distribution in ANPC power cell's states.

- **Power loop parasitic estimation** was carried out to optimize the layout of the GaN DB. Parasitic inductances were estimated by means of a FEA at 100kHz (=$f_{sw}$) in Ansys Q3D Extractor tool.

| Stray Ind. | Value@ 100kHz | Stray Ind. | Value@ 100kHz |
|---|---|---|---|
| $L_p$ | 14.46 nH | $L_n$ | 22.04 nH |
| $L_{1-2}$ | 5.08 nH | $L_{4-3}$ | 3.78 nH |
| $L_{1-5}$ | 5.72 nH | $L_{4-6}$ | 6.15 nH |
| $L_{0-5}$ | 13.93 nH | $L_{0-6}$ | 11.04 nH |
| $L_{2-3}$ | 4.84 nH | | |



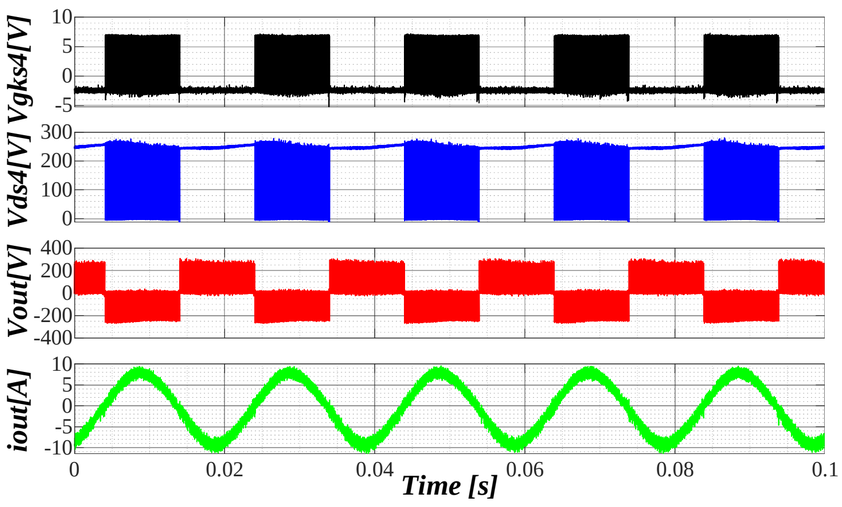




Electric circuit made up of stray inductances related to GaN DB's designed traces.

## RESULTS & DISCUSSION

Preliminary tests were carried out on single-phase ANPC cell which evidence relatively low overvoltages in drain-to-source voltages, due to the minimization of power loop parasitic inductances and to the additional placing of RC snubbers. Gate-to-Kelvin source voltages do not appear so much affected by high-frequency noises, due to the sundering of the driving and the power sections. Output voltage features good symmetry due to the optimized switching loop layout.




Gate-to-Kelvin source (black) and drain-to-source (blue) voltage of S4, output voltage (red) and filtered phase output current (green) at 500VDC.

## CONCLUSION AND FUTURE WORK

In this poster, a methodology of developing power converters is presented. Sundering of power and driving sections constitutes an advantageous solution to simplify the layout, improving conductive paths' routing, increasing layout simmetry and reducing parasitics. Future work concerns the experimental validation of the three-phase power conversion unit.