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A Low-Power, Fast Transient Response Low-Dropout Regulator Featuring Bi-Directional Level Shifting for Sensor Applications †

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Abstract: Wireless sensor network (WSN) is an important component of healthcare. The design of the power management unit for WSN poses significant challenges, as it not only needs to achieve good current efficiency but also requires high power supply rejection (PSR) and good load transient performance. This paper presents a low-dropout regulator (LDO) with low quiescent current and fast transient response to adequately meet the power supply requirements of WSN systems. To ensure system stability and reduce voltage spikes during load transients, an adaptive frequency compensation network is integrated into the circuit. Additionally, the LDO incorporates a level shifter that facilitates bi-directional transmission of voltage signals across different power systems. The proposed LDO is designed and simulated in a 180 nm BCD process. It operates under a wide input voltage range from 0.8 V to 5.5 V, supports maximum load currents of up to 500 mA, and allows output voltages to vary from 0.8 V to 3.6 V by adjusting the feedback resistance. As a result of implementing the adaptive frequency compensation circuit, the overshoot and undershoot voltages at an output voltage of 1 V are measured to be only 23 mV and 5 mV, respectively. Moreover, the LDO achieves a PSR of −83 dB for bias voltage and −91 dB for input voltage at 1 kHz. The level shifter's highest working frequency can reach 20 MHz under supply voltages (V_{in} = 1.65 V to 5.5 V; V_{out} = 3.6 V), thereby enabling high-speed data transmission. Finally, the LDO consumes a quiescent current of 42 μA while incorporating a bandgap reference circuit and other auxiliary circuits.

Keywords: wireless sensor network; low-dropout regulator; adaptive frequency compensation; level shifter

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1. Introduction

Wireless sensor nodes have been widely adopted in various fields, including smart homes, military communications, and medical care, due to their advantages of compact size, low power consumption, high cost-effectiveness, and ease of installation [1,2]. Figure 1 illustrates a wireless sensor network system used for physiological monitoring, where each user wears multiple wireless sensor nodes for physiological signal acquisition. Due to the limited area (≈50 mm × 30 mm) of each node, there are stringent requirements regarding size and power consumption.

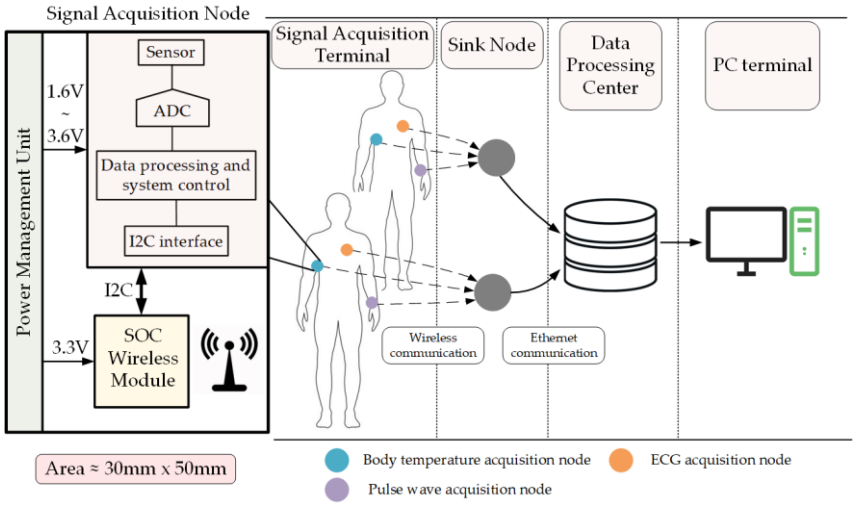

Figure 1. Overall structure of the physiological monitoring wireless sensor network.

The operation of wireless sensor network (WSN) node involves two distinctly different load conditions: light-load operation for sensors and heavy-load operation for transceivers [3]. This requires the power management unit to exhibit good transient performance while also meeting low power consumption and high-power supply rejection ratio (PSR) requirements. Low dropout regulator (LDO) can generate clean, high-precision voltage that are independent of the input voltage. Additionally, they occupy less space compared to switching regulators, as they require fewer external components. All these advantages make LDO the ideal choice for power supply in WSN systems.

In the past, several standard approaches have been adopted to either reduce quiescent current or enhance transient response; however, they could not satisfy all requirements simultaneously. For instance, reference [4] proposed a load transient-enhanced circuit based on an FVF circuit configuration for an LDO that features a quiescent current of only 204 nA. However, being limited to a maximum load current of only 10 mA does not meet the load requirements of WSN nodes. In reference [5], the author proposed a capacitorless LDO that significantly enhances PSR through an adaptive supply ripple cancellation (ASRC) technique. Measurement results indicated that the proposed LDO achieves a PSR of less than −36 dB across all frequencies from 10 kHz to 1 GHz, demonstrating its superior performance and robustness. However, it consumes over 200 μA of quiescent current, resulting in very low current efficiency.

In the wireless sensor node illustrated in Figure 1, a system-on-chip (SoC) wireless control module is configured to connect with the parameter collection module via the inter-integrated circuit (I2C) interface, facilitating seamless parameter collection and transmission. However, different systems often operate at varying supply voltages, which complicates data transfer between them. This situation necessitates the use of level shifters to resolve the issue. Currently, most commercially available level shifters are standalone chips that require careful circuit planning during system design, thereby increasing both design costs and complexity.

To address the issues mentioned earlier, we propose a low dropout linear regulator chip that features level shifting capabilities. This chip not only meets the power supply requirements of wireless sensor networks but also serves as a bridge for signal transmission between systems operating at different voltage levels.

2. Design of the Proposed Low-Dropout Regulator

Figure 2 illustrates the block diagram of the proposed LDO, which primarily consists of an error amplifier (EA), a buffer, a power MOSFET, an adaptive frequency compensation, and a level shifter. The error amplifier ensures the accuracy and stability of the output

voltage. The super source follower (SSF) buffer, along with the adaptive frequency compensation module, contributes to the overall stability of the system. This enhancement guarantees that the output voltage remains stable during transient changes in load current while significantly reducing fluctuations caused by load variations. We utilize NMOS as the power transistor to enhance transient response while minimizing the layout area. Furthermore, to achieve single-chip power supply and level shifting, a level shifting module is integrated into the LDO, facilitating signal transmission between the input voltage (V_{in}) and output voltage (V_{out}) domains.

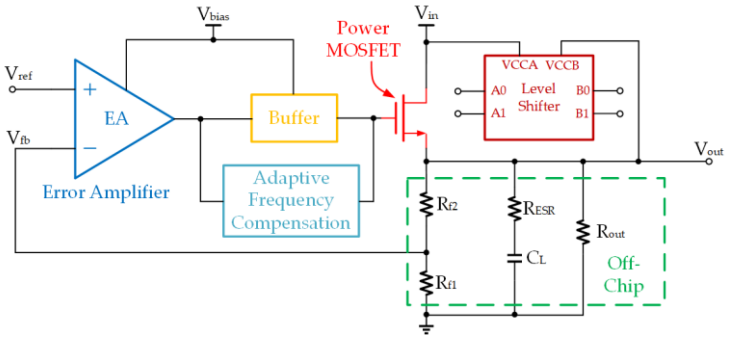

Figure 2. Block diagram of the proposed LDO.

2.1. Super Source Follower

The SSF is designed as a buffer, drawing inspiration from the traditional source follower configuration. To accommodate an output load current of 500 mA, the required power transistor must be sufficiently large, which leads to increased parasitic capacitance at the gate of the power transistor. Additionally, to meet the output linearity requirements, the error amplifier must possess a sufficiently high gain, resulting in a significant increase in its output impedance. If the output of the error amplifier is directly connected to the gate of the power transistor, it would introduce a low-frequency pole that could compromise the system's stability. Therefore, it is essential to place a buffer between the error amplifier and the gate of the power transistor to achieve pole separation and enhance the system's slew rate. This paper utilizes the SSF illustrated in the Figure 3, with its output impedance represented by Equation (1).

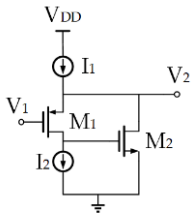

Figure 3. The schematic of super source follower.

$$R_{out}=\frac{1}{(g_{m1}+g_{mb1})g_{m2}(r_{o1}//r_{oI1})} \quad (1)$$

where g_{m1} and g_{m2} represent the transconductance of transistors M_1 and M_2, respectively. g_{mb1} denotes the bulk transconductance of M_1, while r_{o1} and r_{oI1} refer to the output resistances of M_1 and the current source I_1, respectively.

2.2. Adaptive Frequency Compensation

Relying solely on the SSF is insufficient to ensure that the LDO maintains stability under various load conditions. As load current changes, the output impedance at the

output terminal will also vary. With the output capacitance remaining constant, an increase in load impedance will cause the output pole to move toward lower frequencies, thereby reducing the phase margin. To ensure the LDO remains stable during fluctuations in load current, this paper introduces an adaptive frequency compensation circuit built upon the SSF design. The specific design of this frequency compensation circuit is illustrated in Figure 4.

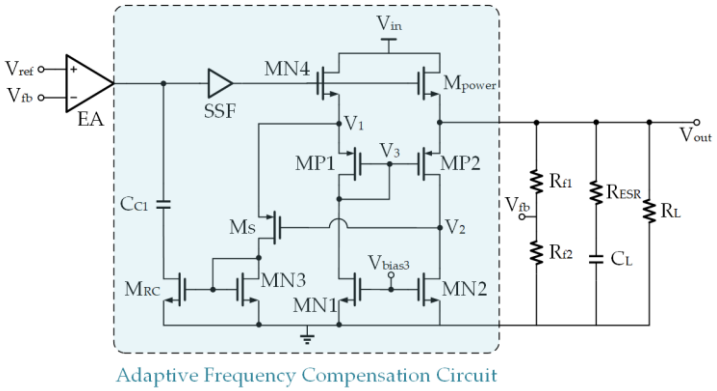

Figure 4. The schematic of the adaptive frequency compensation circuit.

In this circuit, M_{power} acts as the power transistor, while MN4 proportionally replicates the current from the M_{power}. The equivalent resistance of M_{RC}, in conjunction with capacitor C_{c1}, is used for zero frequency compensation within the circuit. Due to the characteristics of the current mirror, when the load current is low, the source voltages of M_{power} and MN4 are equal. However, as the load current increases, the gate voltage of the power transistor and the source voltage of MN4 also rise. To maintain the current through MP1, voltage V_3 will increase, causing MP2 to enter cutoff mode. At this point, the voltage at V_2 decreases, resulting in the conduction of M_{sw}, allowing the current from MN4 to flow through M_{sw}. Consequently, the operating state of the M_{RC} transistor transitions from cutoff to the linear region, reducing its equivalent impedance and producing a zero within the unity gain bandwidth together with C_{c1}.

The Figure 5 illustrates the small-signal model of the LDO after frequency compensation, where the output impedance of the error amplifier is represented as R_1, and the output capacitance is equivalent to C_1. Under the influence of the SSF, the equivalent impedance at the gate of the power transistor is significantly reduced. C_2 represents the equivalent capacitance at the output of the SSF, primarily arising from the parasitic capacitance of the power transistor. To ensure the transient performance of the LDO, a relatively large capacitor C_L (typically on the order of microfarads) is usually added at the output. Additionally, the output impedance R_{out} varies with changes in load current, thereby affecting the system's stability. G_{m1} and G_{m2} represent the transconductances of the EA and the M_{power}, respectively. In the adaptive compensation circuit, the compensation capacitor is denoted as C_{c1}, while R_c is the equivalent resistance of the M_{RC}, which changes with variations in load. Finally, β represents the feedback factor.

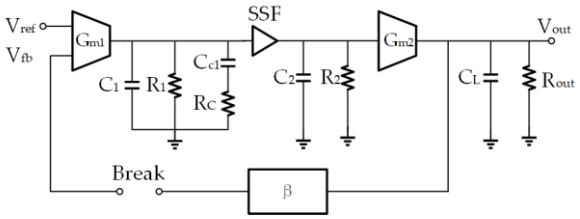

Figure 5. Small signal model of the LDO with adaptive frequency compensation circuit.

Based on the description above and the small signal model, we can derive the open-loop transfer function of the system as follows:

$$T(s)=\frac{\beta G_{m1}G_{m2}R_1R_{out}(1+R_cC_{c1}s)}{(1+R_{out}C_Ls)(1+R_2C_2s)[R_1R_cC_{c1}C_1s^2+(R_1C_1+R_cC_{c1}+R_1C_{c1})s+1]} \quad (2)$$

When the transistor M_{RC} operates in the linear region, the resistance R_1 is much greater than R_c, and the capacitance C_{c1} is significantly larger than C_1, then the transfer function can be simplified as follows:

$$T(s)=\frac{\beta G_{m1}G_{m2}R_1R_{out}(1+R_cC_{c1}s)}{(1+R_{out}C_Ls)(1+R_2C_2s)(1+R_1C_{c1}s)(1+R_cC_{c1}s)} \quad (3)$$

This allows us to obtain the zero and poles of the system, as shown in Table 1:

Table 1. Zero and poles of the compensated LDO.

Parameter	Equation
ωp1	1/R1Cc1
ωp2	1/RoutCL
ωp3	1/RcC1
ωp4	1/R2C2
ωz1	1/RcCc1

The open-loop gain is shown in Figure 6. As the load current decreases, the output impedance R_{out} and the equivalent resistance R_c of the MOSFET M_{RC} gradually increase, which primarily affects the positions of ω_{p2}, ω_{p3}, and ω_{z1} in the frequency response. However, when the load current is very low, M_{sw} turns off, causing M_{RC} to enter the cutoff region. Additionally, when there are significant variations in the load, M_{RC} struggles to remain in the linear operating region and is prone to entering saturation [6]. The combined effects of these factors lead to a substantial increase in the equivalent resistance of M_{RC}, resulting in an unstable state for the system.

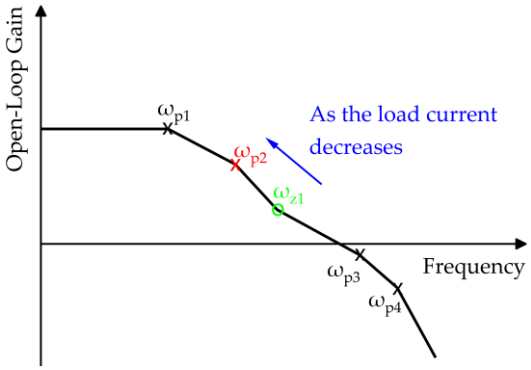

Figure 6. Loop gain of the LDO with adaptive frequency compensation circuit.

Therefore, modifications were made to the circuit in Figure 4 by adding an additional zero compensation at the output of the error amplifier and simultaneously introducing an output feedforward capacitor. Figure 7 shows the complete LDO schematic with the adaptive frequency compensation circuit. The error amplifier is designed as a folded cascode amplifier, and the current mirror PMOS transistors operate in the sub-threshold region to reduce static power consumption and improve DC gain. To minimize layout area and enhance load transient response, NMOS transistor are used as power device in the circuit. Additionally, the circuit employs dual power supply to reduce the dropout voltage.

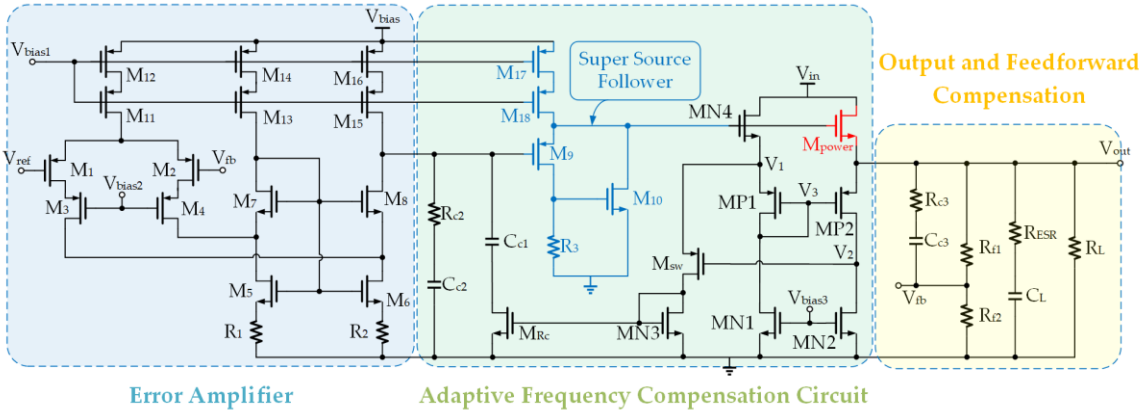

Figure 7. The complete schematic of the proposed LDO.

In conditions of low load current, ω_{z1} and ω_{p3} approximately cancel each other out. At this point, the compensation resistor R_{c2} and compensation capacitor C_{c2} create a zero within the unity gain bandwidth, effectively replacing the positions of C_{c1} and R_c, thereby maintaining the stability of the system. Additionally, the feedforward compensation capacitor C_{c3} and compensation resistor R_{c3} introduce another zero. By adjusting the values of these resistors and capacitors, the zeros can be positioned within the unity gain bandwidth, effectively enhancing both gain and phase, thus improving the overall phase margin of the loop.

2.3. Integrated LDO and Level Shifter

In a multi-voltage system, such as a WSN node or an internet of things (IoT) device, when a lower voltage powered module directly drives a higher voltage powered module, the significant voltage difference may prevent the PMOS transistor in the load unit from turning off completely. This can lead to substantial leakage current and noticeable leakage power consumption. In severe cases, it could even result in the malfunctioning of the chip. Therefore, a level shifter must be inserted between different voltage domains. Thanks to our proposed LDO, which features a wide input voltage range and adjustable output voltage, we have integrated a level shifter suitable for open-drain outputs that supports bidirectional transmission into this LDO, as illustrated in Figure 8. In this block diagram, we connect the input voltage V_{in} to the power supply of side A of the level shifter and the output voltage V_{out} to the power supply of side B. This allows us to achieve both power supply for the master-slave devices and data transfer between them using a single chip, thereby simplifying circuit system design and reducing costs.

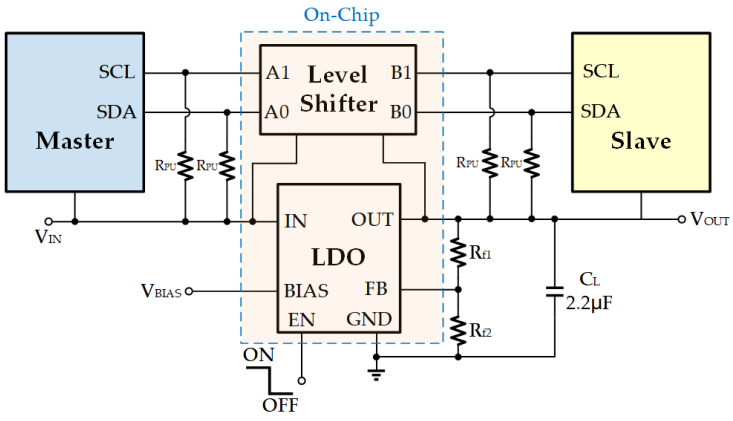

Figure 8. Block diagram of the proposed LDO with level shifter.

3. Simulation Results and Discussion

The proposed LDO is designed on a 180 nm BCD process. Figure 9 shows the layout of this design, with an overall area of 1108 μm × 686 μm. This design includes a bandgap reference, an error amplifier, an adaptive frequency compensation circuit with a super source follower, the power transistor and the level shifter.

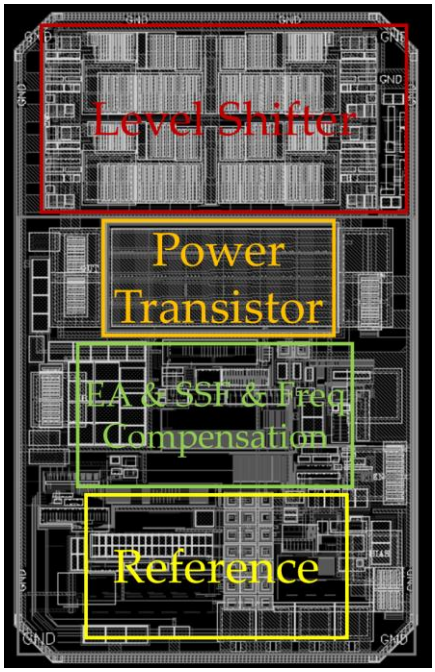

Figure 9. Layout of the proposed LDO.

We set the input voltage range from 1.3 V to 5.5 V, the output voltage at 1 V, and the load capacitance at 2.2 μF for the simulation. Figure 10 illustrates the open-loop frequency response of the LDO under various load conditions. It is evident that changes in load significantly affect stability. Thanks to the adaptive frequency compensation circuit, the phase margin varies between 50° and 67°, indicating that the system can maintain stability. However, this comes at the cost of reduced bandwidth, demonstrating the trade-off between stability and speed.

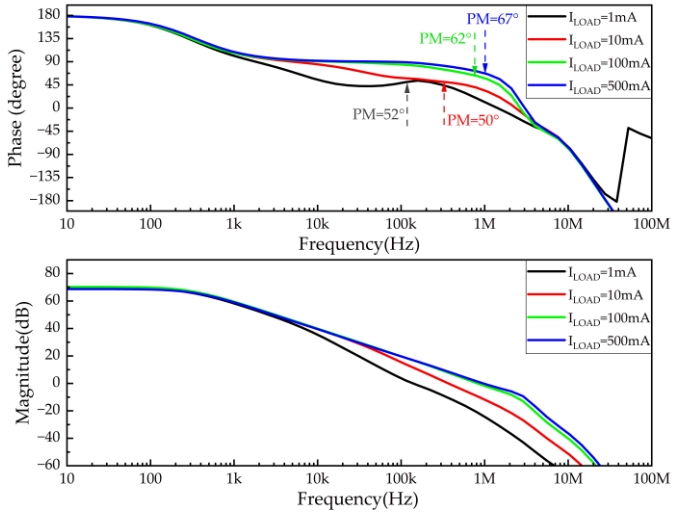

Figure 10. Simulated open-loop gain and phase response at different loads.

The proposed LDO uses an NMOS transistor as the power device and employs dual power supply to reduce dropout voltage, necessitating consideration of the PSR of both V_{bias} and V_{in}. Figure 11 illustrates the simulated PSR performance of the proposed LDO under a load current of 150 mA. Thanks to the design of the common-source and cascode amplifiers along with the feedforward circuit, the PSR of V_{bias} reaches −83 dB at 1 kHz. Additionally, with the effect of the NMOS power transistor, the PSR of V_{in} also attains −91 dB at 1 kHz.

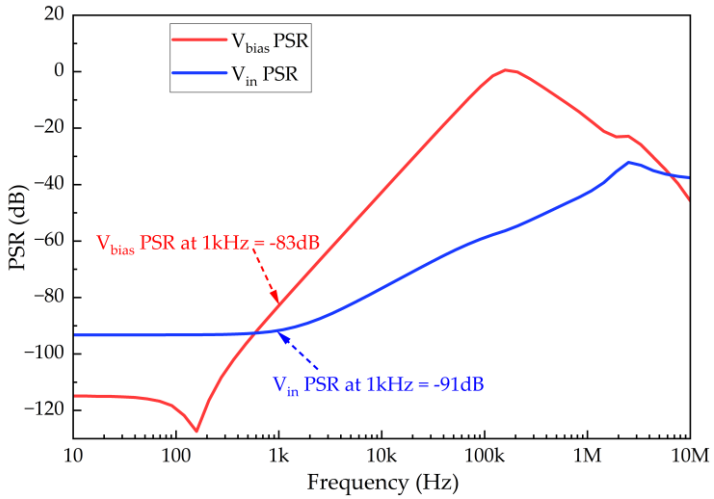

Figure 11. Simulated PSR of the proposed LDO.

The WSN node experiences variations between heavy and light loads during operation, which places high demands on the transient performance of the LDO. Figure 12 presents the transient simulation results when the load changes from 1 mA to 500 mA, with both the rise and fall times set at 5 µs and an output voltage of 1 V. During the load current increase, the maximum voltage swing is 23 mV; conversely, during the load current decrease, the overshoot of output voltage is 5 mV, with recovery times of 12 µs and 25 µs, respectively.

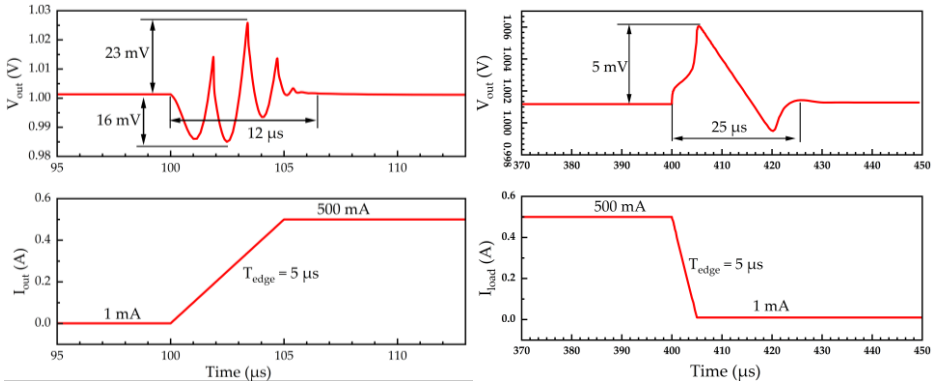

Figure 12. Simulated load transient response of the proposed LDO.

We have functionally integrated a level shifter into the LDO. Figure 13 illustrates the output simulation results of this level shifting module, where the input voltage V_{in} is set at 5 V, with output voltages V_{out} of 3.6 V and 1.8 V. The results indicate that the maximum data rate can reach 20 MHz when voltage translating from 5 V to 3.6 V, and up to 10 MHz when voltage translating from 5 V to 1.8 V.

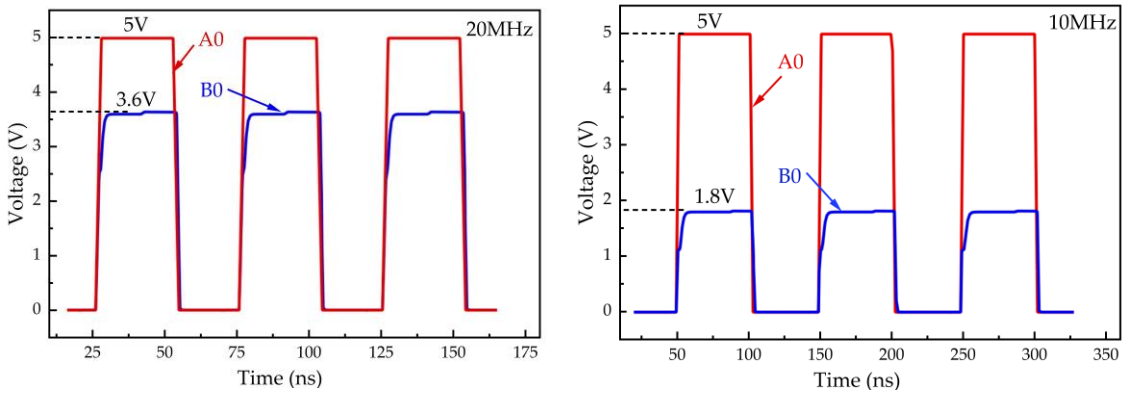

Figure 13. Simulated results of the level shifter with different V_{in} and V_{out}: (**a**) V_{in} = 5 V, V_{out} = 3.6 V; (**b**) V_{in} = 5 V, V_{out} = 1.8 V.

The figure of merit (FOM) in [7] is adopted to evaluate the transient response of an LDO with respect to the change in the load current. The performance comparison with previously reported LDOs is summarized in Table 2.

Table 2. Performance summary and comparison with different LDOs.

Parameter	[8]	[9]	[10]	[11]	This Work
Published date (year)	2020	2020	2024	2024	2024
Technology (nm)	180	180	600	110	180
V_{in} (V)	1.4–1.8	5.5	2.2–5.5	4–4.5	0.8–5.5
V_{out} (V)	1.2	1.5–5.25	1.8–3.3	1.85	0.8–3.6
ΔV_{out} (mV)	20	36	38.6	271	23
C_{out} (μF)	4.7	2.2	1	1	2.2
I_q (μA)	13.5	5.6-35.6	9.6	57	42
$I_{load,\ max}$ (mA)	150	250	150	300	500
$I_{load,\ min}$ (mA)	0.1	NA	NA	NA	1
Line reg (mV/V)	7.785	10.20	1	1	0.62
Load reg (mV/mA)	0.0750	0.1120	0.06	0.00267	0.0018
V_{in} PSR @ freq(dB)	−30 dB @100 Hz	−70 dB @1 MHz	−71 dB @1 KHz	−22 dB @1 MHz	−91 dB @1 KHz
V_{bias} PSR @ freq(dB)	NA	NA	NA	NA	−83@1 KHz
FOM [1] (ps)	104	7.10	16.47	171	8.5

[1] $FOM = C_{out}\Delta V_{out}I_q/I_{load,\ max}{}^2$.

4. Conclusions

This paper proposes a low-power LDO circuit with fast transient response and high PSR specifically designed for wireless sensor network nodes. The proposed LDO utilizes an adaptive frequency compensation circuit along with additional zero and feedforward compensation to address the design challenges of stability and load transient response. During the transient change of load current from 1 mA to 500 mA within 5 μs, the maximum swing of the output voltage is only 23 mV (with an output voltage of 1 V), and it can recover stability within 25 μs. Thanks to the use of a folded cascode error amplifier and NMOS transistor as power device, the circuit achieves sufficient loop gain while maintaining good power supply rejection performance. Functionally integrating a level-shifting module into the LDO expands its application range, simplifies external design, and meets the demands for system integration and miniaturization, showing better prospects in applications such as sensors and IoT devices.

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