DESIGN OF EFFICIENT PHASE LOCKED LOOP FOR LOW POWER APPLICATIONS

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***Abstract*— The phase-locked loop is a technique that has contributed significantly to technological advancements in many applications in the ever so fast-evolving digital era. In this paper, a PLL is designed using 90 nm CMOS technology node with 1.8V supply voltage. It features a PLL design with minimum power consumption of 194.26µW with better transient analysis and DC analysis in an analog-to-digital environment. The proposed PLL design provides the best solution for many applications where a PLL is required with high performance but has to be accommodated in less area and low power consumption than state-of-the-art methods. This PLL not only works at high speed, but also makes whole system works at low power in a very effective manner which suits for the present digital electronics circuits.**

Keywords*— *Phase locked loop (PLL), Phase frequency detector/Charge pump (PFD/CP), Low pass filter (LPF), Current starved voltage-controlled oscillator (CSVCO), Analog Digital environment (ADE).

I. INTRODUCTION

The current era is all about compact battery devices used in electronic devices. A PLL is used in all SOC devices where circuitry generates a system clock signal. Basically, a PLL has a feedback loop that controls the phase of the output signal with the input signal along with phase error.

Phase Frequency Detector blocks can be implemented with D, SR, or JK flip-flops. Figure 1 shows the block diagram of a PLL. It mainly consists of four blocks called PFD (phase frequency detector), Charge Pump with Low Pass Filter, a Voltage controlled oscillator (VCO) to provide oscillations and a Frequency Divider [1].

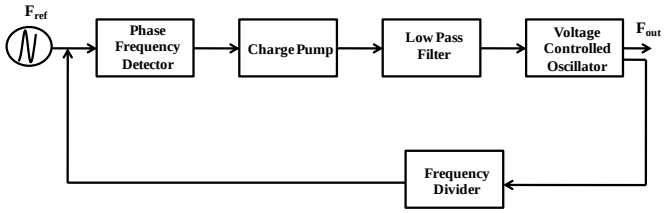


Fig.1. Block diagram of PLL.

II. METHODOLOGY

Previously, a multiplier was used as an analog phase detector, but it had a limited blocking range and with a phase error of more than 90° where the output voltage is reduced. A digital phase detector was implemented where the mean value is proportional to the phase error. Mainly X-OR gate was used as a phase detector which is linear, but if it were in phase and the error was greater than 180° then it would lose its linearity. Consequently, the phase-frequency detectors are designed to detect phase and frequency differences, which increases the speed of PLL.For the LPF (low pass filter) design, the first order low pass filterwas designed, but it would introduce ripples as the control voltage jumps high when current is injected from the charge pump. To solve this problem, a second-order low-pass filter can be designed to suppress the generated ripple.Firstly, VCOs (voltage-controlled oscillators) were designedusing LC oscillators or ring oscillators.But ring oscillators are notstable as they let the switching characteristics of logic gates fluctuate by +/- 20% and the disadvantage of LC oscillators was more matrix area.Therefore, the currently hungry VCOs are realized in our proposed design.

The PLL works in three states: Free Running state, Capture state and Phase Lock state. As the name suggests, the free-running state refers to the phase in which no input voltage is present. As soon as the input frequency is applied, the VCO starts switching and starts producing an output frequency to be compared, this stage is called the capture state.

The frequency comparison stops as soon as the output frequency equals the input frequency. This phase is known as the phase-locked state. PLL is a convenient circuit block widely used in wireless applications, electronics, from cell phones to radios, televisions, etc. Wi-Fi. Fi routers, areas like FM demodulators, AM demodulators, frequency synthesizers and more recovery etc.

III. DESIGN AND IMPLEMENTATION

The proposed design of 90 nm PLL using GPDK library in cadence virtuoso consists of all the blocks of a Basic PLL. In this design the number of transistors is reduced when compared to the existing designs in [1] and [2]. Due to this the area is reduced. Also, the reduced transistors lead todecreased usage of the power consumption and cost. The design of blocks of the proposed PLL are shown and discussed below.

A. Phase Frequency Detector

The phase frequency detector mainly consists of two D- flip flops and Nand gates. The block diagram of the PFD is shown below in Figure 2. The main purpose of a PFD is to compare the phase and frequency of the input signal with the feedback signal. It has two output signals, up and down.

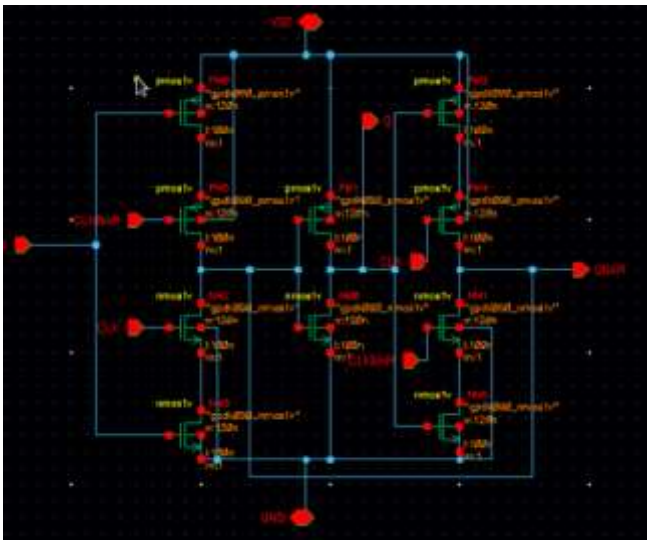


Fig. 2. Schematicof D flip flop.

The design of the low power edge triggered D-Flip flop with 1.8 V is designed with reduced number of transistors and the respective output waveforms are shown in Figure 2. The proposed schematic of PFD block is shown in Figure 3 with a smaller number of transistors.

B. Charge Pump and Low Pass Filter

The charge pump block converts the output of PFD block into a voltage that controls the VCO. When the UP signal is high, the positivecurrent IPDI flows through the circuit and increases the control voltage, When the downstream signal goes high, a negative IPDI current flows through the circuit, that reduces the control voltage. The output current of the charge pump [4] is given below Eq.(1):

$$I_{PDI} = K_{PDI}\, X\, \Delta\emptyset \qquad (1)$$

$$Where\ K_{PDI} = \frac{I_{PUMP}}{2\pi}$$

$$\Delta\emptyset = \emptyset_{IN} - \emptyset_{REF}$$

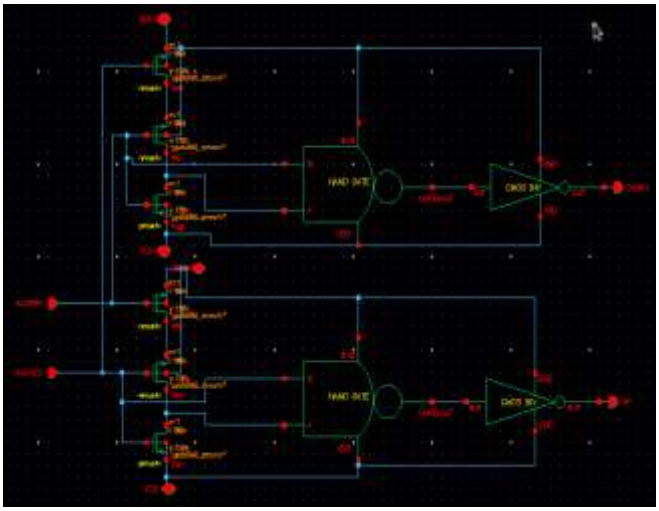


Fig. 3. Schematic of Phase frequency detector

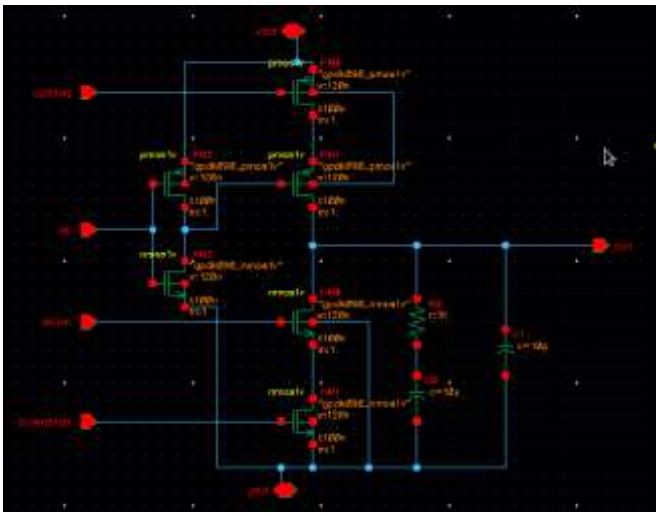


Fig. 4. Schematic of charge pump with low pass filter

The control voltage of VCO is given in Eq. (2),

$$V_{ctl}VCO = Kf\ X\ IPDI \qquad [2]$$

The low pass filter converts the charge pump current into voltage and the frequency of the VCO depends on the output of the LPF. When the charge pump current is positive, the oscillation frequency increases otherwise,

it decreases. Figure 4 shows the implementation of Charge pump along with low pass filter.

C. Voltage controlled oscillator

The implementation of a low current VCO circuit that is like a simple ring oscillator with an PMOS and NMOS transistor is done. This limits the current that passes through each inverter hence named as low current VCO. The inverter stage is implemented as shown in [7], [4].The schematicof CSVCO is shown in Figure 5.

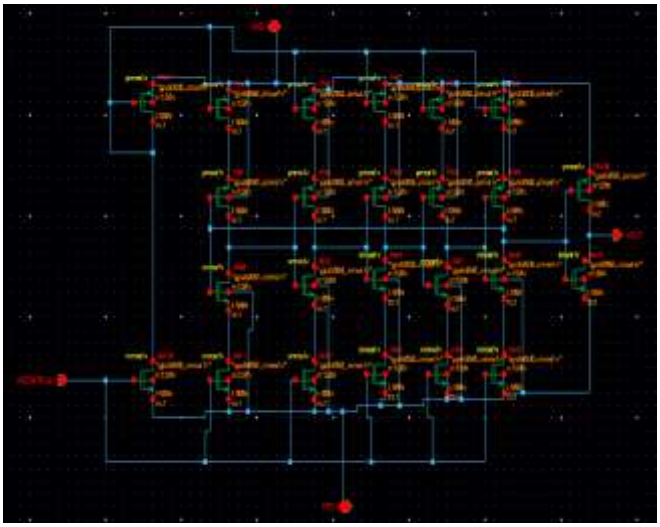


Fig 5. Schematic of Voltage controlled oscillator

D. Frequency Divider

The output of the VCO is provided to the PFD via the frequency divider circuit. The frequency of the VCO output signal is divided by two by this counter block. Two D flipflops are used to implement the counter circuit as shown in Figure 6.

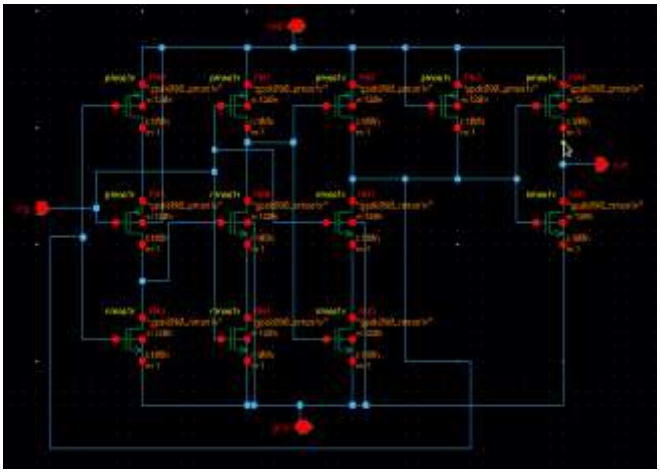


Fig6. Schematicof frequency divider

IV. RESULTS AND OBSERVATIONS

The design of an PLL is done in cadence virtuoso tool by Analog design environment using GPDK 90nm. Here the transient and dc analysis of proposed PLL and its blocks is discussed. A reference signal and clock feedback signal are given as input to the PFD with output as Up and Down Signals. The output of charge pump is given to VCO which acts as a Voltage control signal and the output of VCO is given to Frequency Divider where the frequency is N/2 which is feedback signal given to PFD. The Figure 8 shows the transient and DC analysis of the PLL.

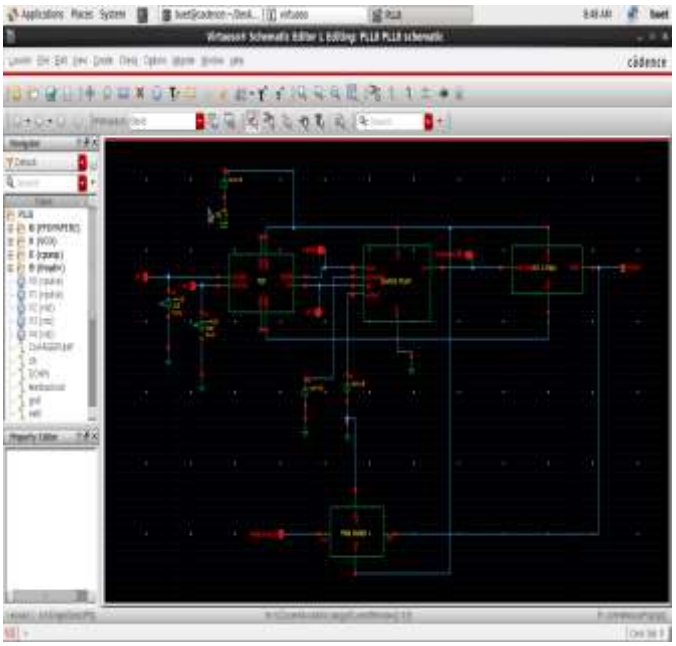


Fig 7. Architecture of Proposed PLL

The Figure 7 shows the proposed architecture of PLL. Here the use of a novel design for PFD and charge pump is used for reducing the power usage of whole system.

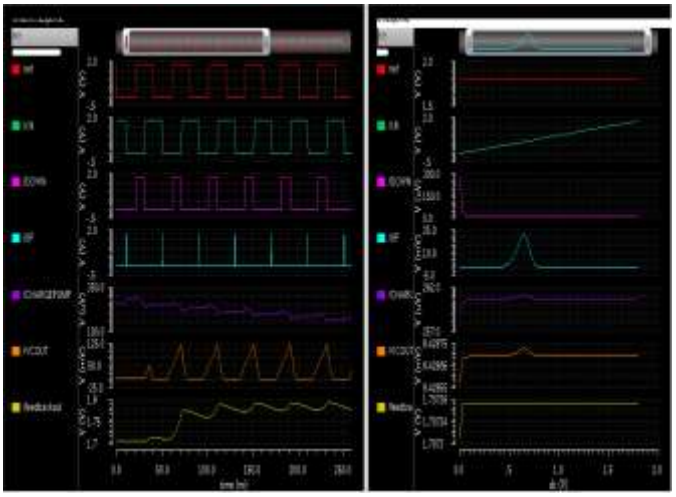


Fig 8. Transient analysis and DC analysis of Proposed PLL

Figure 8 shows transient and DC analysis of proposed PLL that verifies the working of the PLL in effective way. This not only shows the output PFD i.e., up, and down signals that acts according to the clock signal but also showcasethe output waveforms of the charge pump [14] that varies according to the input signals. When both the input signals are high then the output of charge pump is high and when both input signals are low then there is a drop at the output signal of the charge pump, which is given as input to the VCO.

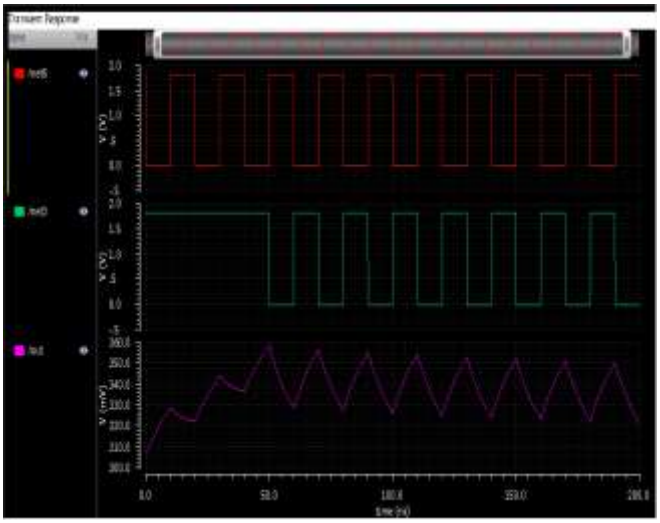
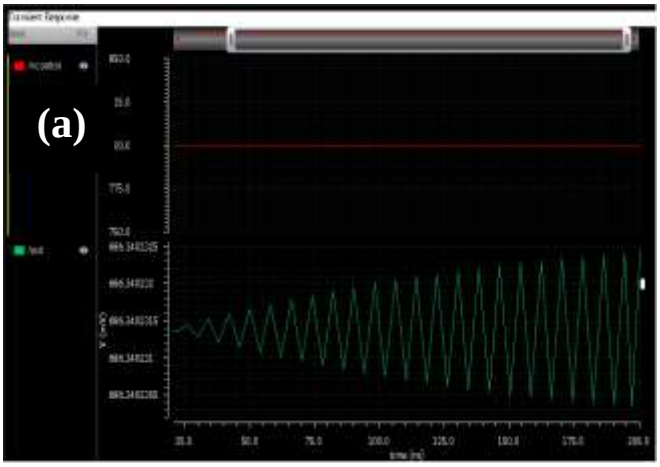


Fig 9. Output Waveforms of Charge Pump



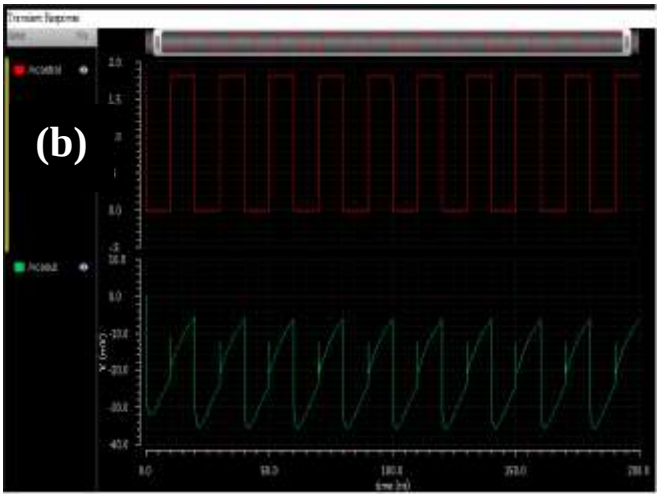


Fig 10.(a) Output waveforms of VCO with $V_{control}$signal(b) Output waveforms of VCO with Input signal

The output waveforms of VCO are shown in figure 10 with respect to the input clock signal. Whereas the output of frequency divider is shown below in Figure 11.

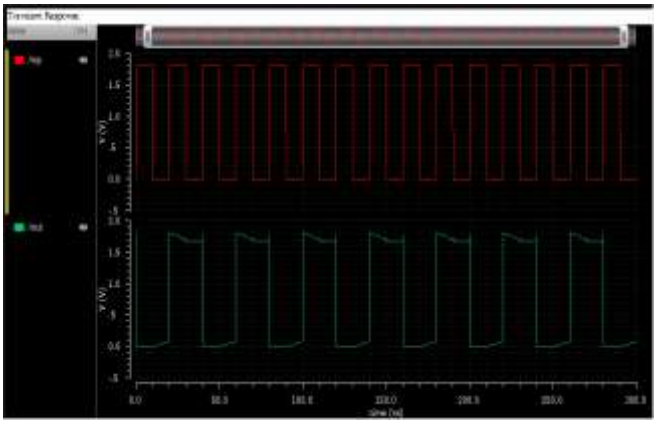


Fig 11. Output wave forms of Frequency Divider

The DC total power analysis plot of the PLL is shown below Figure 12.

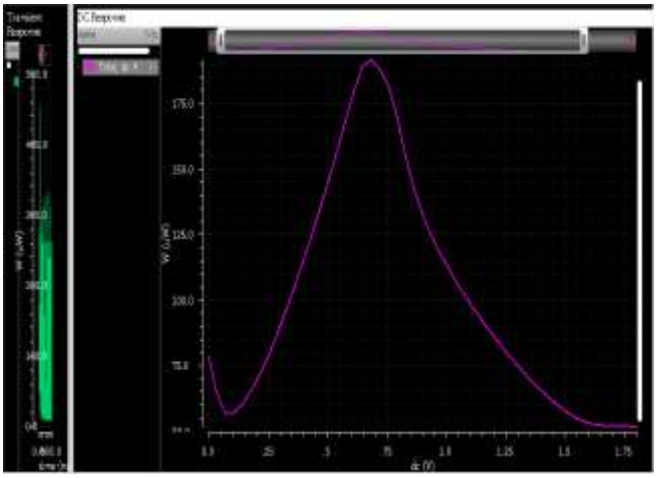


Fig 12. The plot of DC total power analysis

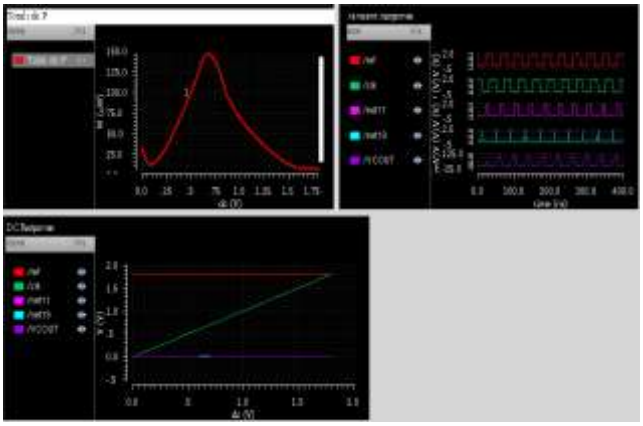


Fig 13. DC power analysis

The results of proposed work are better than results of [1]in terms of power consumption and number of transistors used to design PLL, where power consumption is many times less than [1]. The comparative analysis of various parameters is presented in Table 1.

Table 1. Parametric Analysis

Parameters	Traditional PLL	Existing PLL [1]	Proposed PLL
Number of transistors	112	56	48
V dd	-	1.8 V	1.8 V
Operating frequency	-	1GHz	1GHz
Power Consumption	-	4.2mW	194.24 µW
Total Power Consumed	High	Medium	low
Technology	180nm	90nm	90nm

Here the comparative analysis of different parameters is shown. The parameters such as number of transistors used in design of PLL, supply voltage, operating frequency power consumedare used to implement PLL are analysed above. From the analysis the proposed PLL design has 14% decrease in number of transistors with reduced area and 1000 times less power consumption. So, the proposed PLL can be used effectively used in low power digital electronic applications and compact devices.

V. CONCLUSION

A design of PLL using cadence virtuoso tool in analog design environment by using GPDK 90nm technology with 1.8 V DC supply is done. The simulation work presents a reduced number of transistors with reduced area in proposed design with very low power consumed at DC voltage of 1.8 V. The Total Power Consumed by the proposed PLL design is 194.24micro-Watts. As we know that the power consumed, and sizing of the transistors and selecting the power supply voltage at different levels may vary the total power consumed with respectively. This not only allows the working of PLL at high speed, but also supports working at low power which makes it very effective for low power applications.

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