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# Single-Layer Parity Generator and Checker Design Using XOR Gate in Quantum-dot Cellular Automata

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## INTRODUCTION & AIM

Quantum-dot Cellular Automata (QCA) is a promising nanotechnology developed to overcome the limitations of CMOS, such as high-power consumption, size scaling constraints, and low integration density. QCA leverages quantum dots and their unique tunneling phenomena to create efficient and highly compact logic design nano circuits.

- **Quantum dots** are nanoscale regions being semiconductor tiny structures confining electrons. The four quantum dots arranged in a square shaped QCA cell, holding two electrons to encode binary data.
- **QCA wire** is a sequence of cells transmitting data.
- **Majority Voter (MV)**: A gate providing the majority value of three inputs.
- **Clocking Phases**: Four phases (switch, hold, release, relax) ensuring controlled data flow throughout the circuit.

The aim of the QCA-based parity circuit is to design a dual-tasking 3-bit parity generator and checker that ensures error detection in communication systems with enhanced energy efficiency and reduced fabrication complexity. By leveraging a modified majority voter (MMV) based XOR gate, the circuit achieves dual functionality in a single design, addressing both parity generation and checking tasks.

## PROPOSED WORK

A parity bit is an additional bit added to binary data to detect errors during data transmission. In an even parity generator, the parity bit *PG_out* is set to 1 when the total number of 1's in the input bits A, B, and C is odd, ensuring an even count of 1s. Otherwise, *PG_out* remains 0. This relationship is expressed mathematically in **Eq (1)**:

$$PG\_out = A \oplus B \oplus C \quad (1)$$

where $\oplus$ denotes the XOR operation. The corresponding logic table is shown in **Table 1**.

For error detection, a parity checker circuit ensures that the received four-bit message (inputs P, Q, R, and PG_in) contains an even number of 1s. If this condition is violated, the parity checker outputs an error signal. The relationship is defined in **Eq (2)**:

$$PC = P \oplus Q \oplus R \oplus PG\_in \quad (2)$$

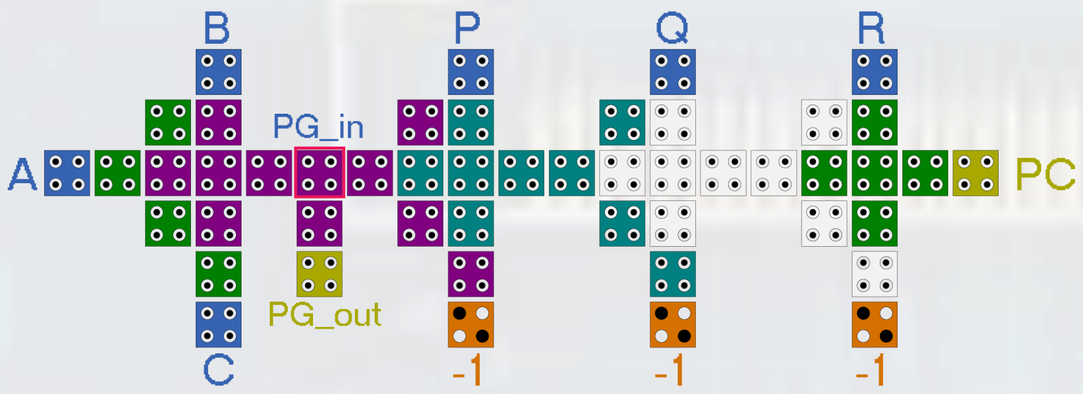



**Fig. 1** QCA layout of proposed circuit

In this work, efficient XOR gates are employed to construct both the parity generator and checker using four modified majority voters in QCA, avoiding crossovers and minimizing fabrication complexity. The proposed design is well optimized for QCA implementation using **QCADesigner 2.0.3** tool.

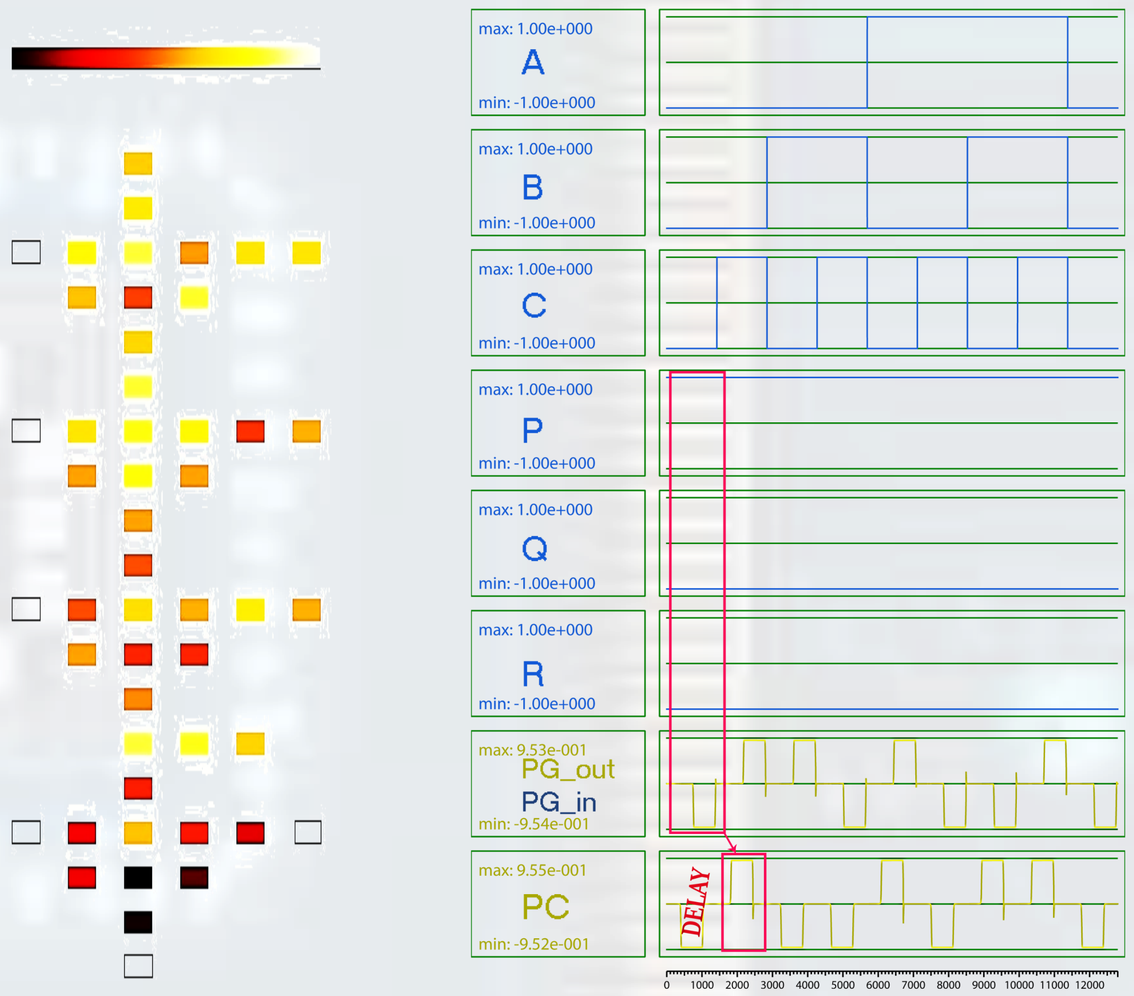
- The parity generator is designed as a 3-input XOR gate, taking inputs *A*, *B*, and *C* to output *PG_out*.
- The parity checker is implemented with three 2-input XOR gates, combining inputs *P*, *Q*, *R*, and *PG_in* to generate the output *PC*.

Figure 1 depicts the circuit layout, where *PG_in* and *PG_out* share the same QCA wire, ensuring uniform polarization. The circuit consists of **49 QCA cells**, requiring a total area of **0.07 μm²**, achieves an overall latency of **1.25 clock cycles**.

- The parity generator uses **15 cells**, occupying **0.03 μm²** of total area.
- The parity checker employs **35 cells**, requiring **0.04 μm²** of total area.

## RESULTS & DISCUSSION

In the context of the proposed dual-tasking QCA layout for the parity checker, the inputs P, Q, and R are used to evaluate the functionality of the parity checking circuit. The specific case of P=1, Q=0, and R=0 is considered during simulation to test how the circuit responds to different input combinations and to ensure that it correctly computes the parity based on these inputs. The parity checker is expected to determine the parity of the inputs and produce the correct output (PC) following the Eqs. (1)- (2). This thorough testing is crucial for confirming the reliability and correctness of the circuit design.




(a) (b)

**Fig. 2** Results of proposed circuit (a) energy hotspot at 0.5 $E_k$, and (b) simulation result

- During operation, this suggested nano circuit dissipates 18.98 meV as leakage energy and 4.88 meV as switching energy at 0.5$E_k$ and 1 K temperature while simulating the circuit using **QCAPro** tool. Hence the total energy was recorded as 23.86 meV using tool.
- During simulation it has been recorded that the proposed circuit has **average output polarization (AOP)** as 0.953 for PG unit and 0.955 for PC unit, which are quite bit higher than any other relevant designs.
- The proposed circuit uses 4 logic gates without any crossover and hence it has the **Figure of Merit (FoM)** as 25 units.
- It demonstrates 86% energy efficiency as well as 59% area efficiency compared to the latest reported QCA-based parity checkers, thus exemplifying a significant advancement in nanocomputing.

## CONCLUSION & FUTURE SCOPE

This research not only constructs a scalable parity generator and parity checker as dual-tasking single circuits employing an optimized XOR gate using QCA technology, but it also conducts a comparative study of multiple existing circuit designs. When compared to existing designs, the proposed circuit yields better result in most of the design parameters. This work also examined the energy dissipation and cost functions of the proposed circuit for better performance evaluation. It dissipates 23.86 meV of energy in particular, which is highly acceptable in QCA technology and the values of the cost function are quite appropriate. The suggested circuit is expected to be a good element for applications in nano-communication and nano-computing architectures.