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Capacitive Behavior of Poly-Si Thin Films in TFTs: Optimizing Device Performance through 2D Numerical Modeling

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INTRODUCTION & AIM

•Low-Temperature Polycrystalline-Silicon (LTPS) TFTs are crucial for microelectronics, optoelectronics, and large-area displays (like active-matrix organic light-emitting diode displays) due to their high carrier mobility.

•However, LTPS films contain a high density of defects, particularly grain boundaries (GBs), which trap carriers, reduce mobility, and impact device characteristics like capacitance-voltage C(V) curves.

•Previous work addressed the quasi-static capacitance, but the high-frequency C−V behavior needed further investigation.

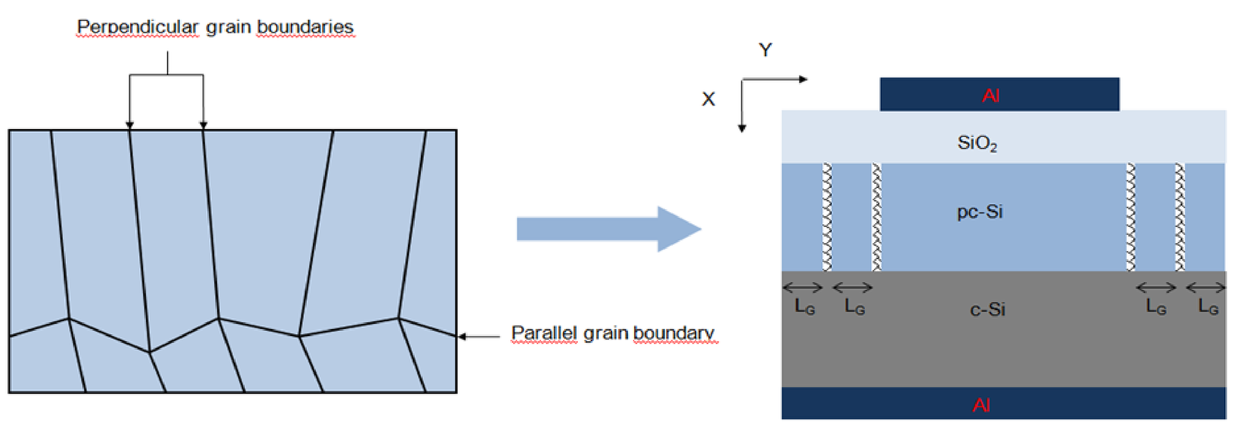
•**AIM:** To develop a 2D numerical simulation code to understand the high-frequency capacitance behavior of the Al/SiO_2/poly-Si structure as a function of the granular structure (number of grain boundaries, grain size, and layer thickness) and oxide thickness.

METHOD

Studied Structure:

•The polysilicon film is modeled with a columnar structure.

•It is composed of identical single-crystal grains (L_G=200 nm) separated by grain boundaries (GBs), which are highly defective regions.



The 2D schematic cross-sectional structure of the Al/SiO_2/poly-Si system

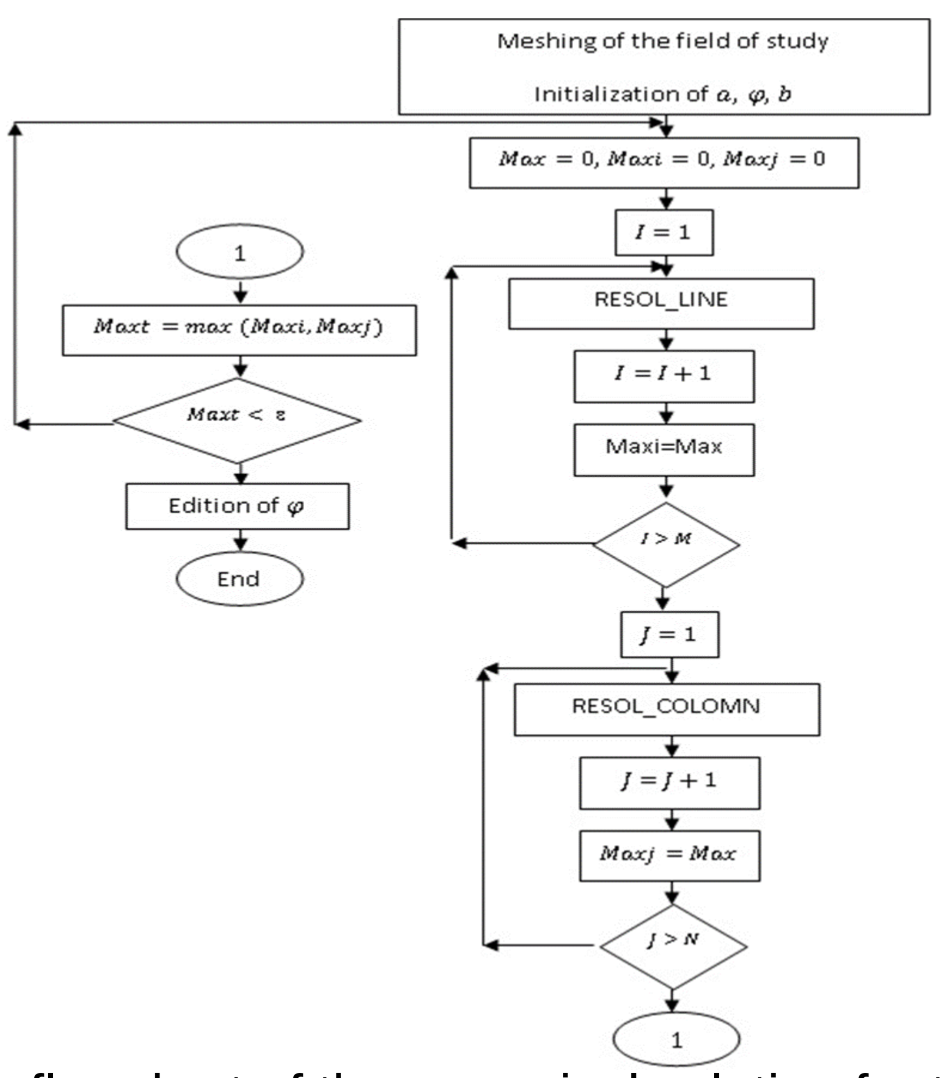
•A custom 2D numerical simulation code was developed based on the solution of the Poisson's equation:

$$div\left(\varepsilon\,\overrightarrow{grad}\,\varphi\right) = -q\left(p - n - N_A^- + N_D^+ + \sum N_T\right)$$

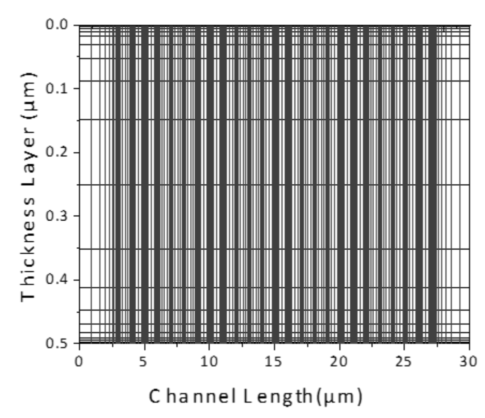
•The high-frequency capacitance $C(V_G)$ is calculated from the following relation:

$$C = \frac{dQ_m}{dV_G}$$

•The simulation determines the behavior of the active layer by applying a transverse gate voltage (V_G) across the SiO_2 layer.



The flowchart of the numerical solution for the 2D Poisson equation

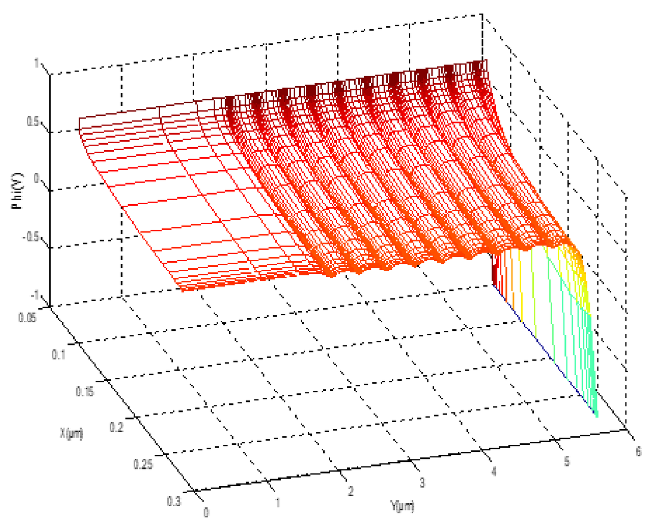


2D-Mesh of poly-Si layer

RESULTS & DISCUSSION

I. Layer at Thermodynamic Equilibrium

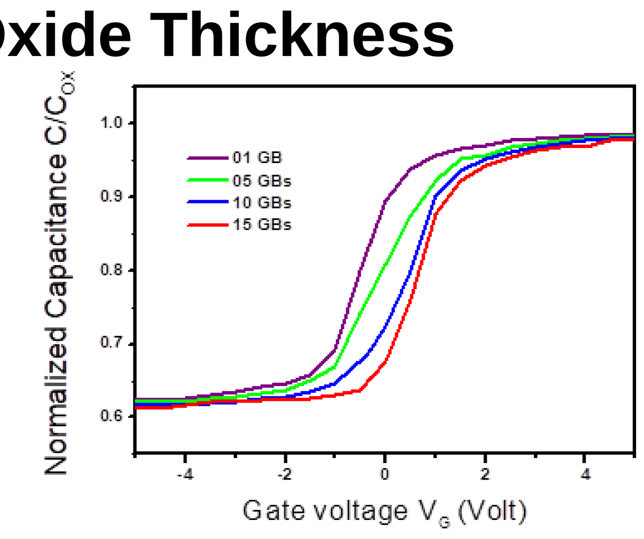
The localized density of states in the GBs traps free carriers, creating a height potential barrier surrounding the grain boundaries when the crystallites are depleted.



II. Impact of Granular Structure and Oxide Thickness

•**Impact of Number of Grain Boundaries (N_{GB})**

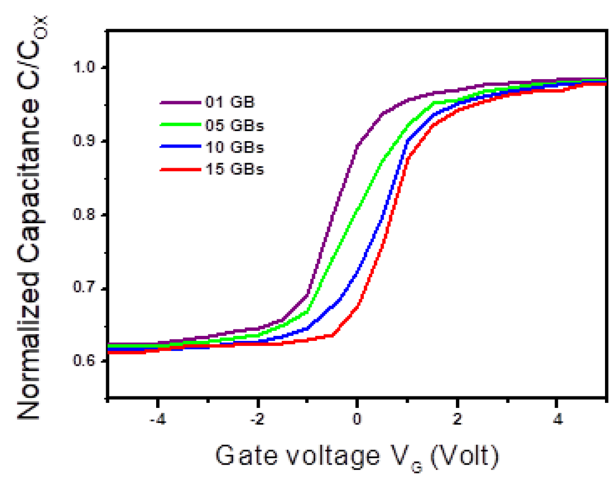
✓ An increase in N_{GB} increases V_T of the high-frequency capacitance.



• **Impact of Layer Thickness (L_C) and Grain Size (L_G)**

✓ Increasing L_C and L_G leads to an increase in V_T

○ **Discussion:** The increase in VT is due to the presence of GBs, which act as potential barriers and restrict the flow of charge carriers.

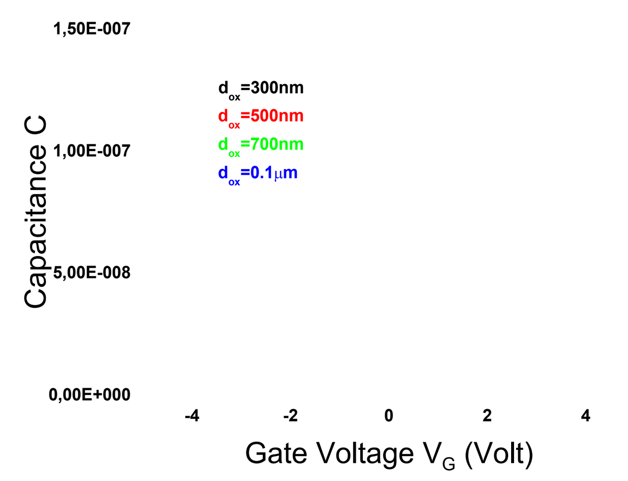


• **Impact of Oxide Thickness (d_{OX})**

✓ The increasing of the granular structure increases V_T.

✓ the presence of GBs in the channel are primarily responsible for the scattering of majority carriers.

✓ It creates a potential barrier that restricts the flow of charge carriers from grain to grain



CONCLUSION

•The study demonstrated that the capacitive effect of poly-Si layers is strongly related to their granular structure (N_{GB}, L_G, and L_C).

•The threshold voltage (V_T) is very sensitive to the number of grain boundaries and also depends on the layer thickness and grain size.

•To achieve the best performance for poly-Si TFT active layers, the solution is to:

✓ Increase the grain size (implying fewer grain boundaries).

Reduce the Density of States (DOS) content at the grain boundaries.

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