ASEC 2025 Conference

The 6th International Electronic Conference on Applied Sciences

09–11 December 2025 | Online

MDPI

Impact of Operating Conditions on the Reliability of SRAM-based Physical Unclonable Functions (PUFs)

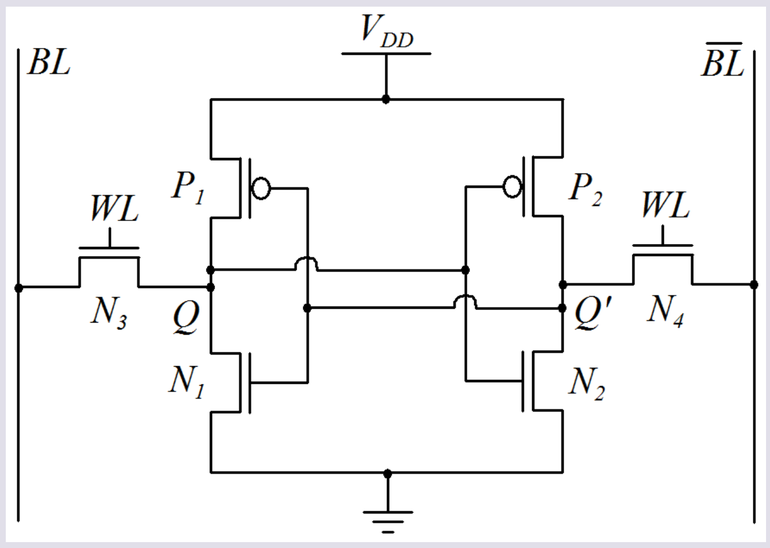
Marco Grossi, Martin Omaña, Simone Bisi, Cecilia Metra, Andrea Acquaviva
Department of Electrical Energy and Information Engineering "Guglielmo Marconi" (DEI), University of Bologna, Bologna, Italy

INTRODUCTION & AIM

Physical Unclonable Functions (PUFs) can be adopted to generate authentication passwords and cryptographic keys exploiting the small variations of the device parameters introduced during the manufacturing process. A PUF device is considered reliable when it generates always the same response when enquired with the same challenge, even in presence of noise and variations of temperature and power supply. The PUF reliability is of paramount importance, since the generation of a wrong signature results in failed authentication with an impact on the system availability. This work evaluates the impact of different operating conditions, such as noise, power supply voltage and temperature, on the reliability of a SRAM PUF.

METHOD

The SRAM PUF generates a unique response, based on the outputs that SRAM cells feature at power-on. The structure of a SRAM cell implemented in CMOS technology is shown in the figure below.



SRAM PUF with 250 SRAM cells.

SRAM cell in 32nm CMOS technology.

Electrical level simulations with LTSpice.

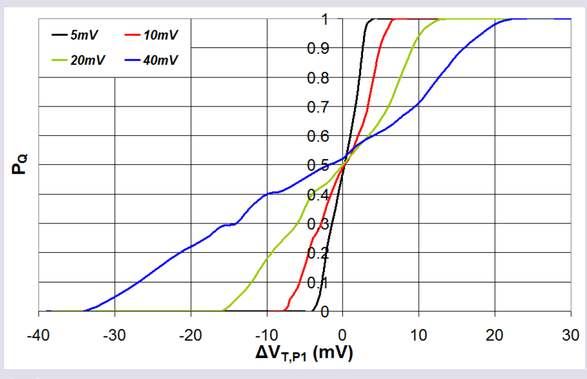
The transistor technological parameters were set as L=32nm, W_n=32nm, W_p=64nm. The nominal operating conditions were set as V_{DD}=1.0V, T=27°C. The technology parameters dispersion due to the manufacturing process was modelled by randomizing the transistor threshold voltages using a Gaussian distribution (average values $V_{T,N}$=493mV and $V_{T,P}$= –491mV).

The impact on the PUF reliability was evaluated under the following conditions:

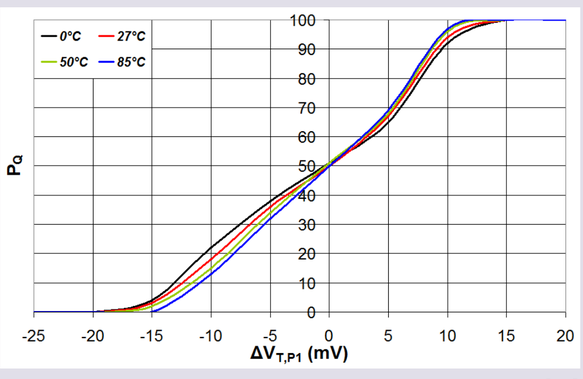
- Different values for the transistors threshold voltage dispersion.
- Different values of the electrical noise level $V_{PP,noise}$.
- Different values of the temperature T.
- Different values of the power supply V_{DD}.

RESULTS & DISCUSSION

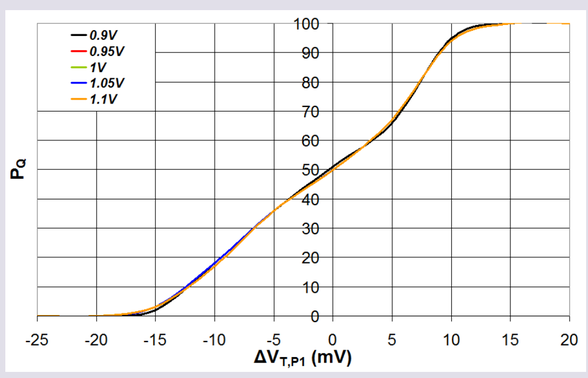
The probability that a SRAM cell stores a logic 1 at node Q at power-on (P_Q) was evaluated as function of the threshold voltage mismatch between the transistors P_1 and P_2 ($\Delta V_{T,P1} = V_{T,P1} - V_{T,P2}$) for different values of: the electrical noise level $V_{PP,noise}$ (A), the temperature T (B), the power supply V_{DD} (C).



(A)



(B)



(C)

Tolerance	Reliability
5%	64.41%
10%	79.67%
15%	84.03%
20%	90.02%

$V_{PP,noise}$	Reliability
5mV	94.76%
10mV	89.17%
20mV	79.67%
40mV	64.5%

Temperature	Reliability
0°C	78.54%
27°C	79.67%
50°C	80.52%
85°C	82.51%

V_{DD}	Reliability
0.9V	79,91%
0.95V	79,66%
1.0V	79,67%
1.05V	79,68%
1.1V	79,73%

The electrical noise level ($V_{PP,noise}$) produces the highest impact on P_Q, while the impact of variations of temperature was lower and the impact of variations of the power supply was negligible.

The reliability metric of the SRAM PUF was evaluated for a 64-bit response, 10000 challenge-response pairs, and 1000 responses for each challenge. The simulation results are presented in the tables, as function of the technology parameters tolerance, the noise level, the temperature, and the power supply.

CONCLUSION

The reliability of a SRAM PUF was evaluated as function of different parameters by means of LTSpice simulations. The results have shown that the PUF reliability is mostly affected by the technology parameters tolerance and the noise level, while the impact of temperature is lower and the impact of power supply is negligible.