ASEC 2025 Conference

The 6th International Electronic Conference on Applied Sciences

09–11 December 2025 | Online

MDPI

Practical Approach for Acquiring the Hall–Huray Surface Ratio Using HFSS Simulations and VNA Measurements

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INTRODUCTION & AIM

High-speed PCBs require accurate modeling of transmission lines to ensure signal integrity at multi-GHz data rates.
FR4 is still widely used due to low cost, but its surface roughness and dielectric properties greatly affect losses.

Problem
The Hall–Huray Surface Ratio (HHSR) is a key parameter for conductor-roughness loss models, but it is usually obtained by costly or complex methods (profilometers, micrographs, advanced numerical fitting).

Aim
Propose a practical and automated methodology to determine the Hall–Huray Surface Ratio for copper conductors on FR4 PCBs by combining HFSS 3D Layout simulations with Optimetrics, and VNA measurements using a WavePulser 40iX with time-domain gating.

Key idea
Instead of directly measuring microscopic roughness, tune HHSR in simulation until the simulated losses match measured S-parameters, yielding an effective and repeatable value for design.

METHOD

Modeling

FR4 was modeled using the **Djordjevic–Sarkar wideband Debye model**, ensuring accuracy over the full high-frequency range and allowing stable dispersion behavior up to 20–40 GHz.
Copper conductor losses were represented using the **Huray "snowball"** model, with a fixed particle radius of 0.5 μm, consistent with low-profile copper typically used in high-speed PCBs.
The **Hall–Huray Surface Ratio (HHSR)** was chosen as the key roughness parameter, and its value was determined by matching simulated and measured transmission characteristics.
This modeling approach enables a practical way to infer copper roughness without requiring profilometry or destructive analysis.

HFSS Electromagnetic Setup

The real 6-layer PCB was imported in .edb format, preserving stackup, trace widths and copper thickness.
The model included 50 Ω and 100 Ω microstrip lines (≈74.6 mm), with fabrication details such as copper roughness and etch factor = 2.7. **HFSS 3D Layout** was configured with wave ports and a frequency sweep up to 20 GHz.
Using Optimetrics, HHSR was swept from 1 to 9, generating S-parameters and TDR curves for comparison with measurements.

VNA/TDR Measurements

Measurements were performed using the **WavePulser 40iX**, which integrates VNA, TDR and TDT up to **40 GHz**, enabling broadband characterization of insertion and return loss. SMP connectors and fixtures were removed through time-domain gating, eliminating unwanted reflections from cables and adapters (total propagation delay ≈ 75 ps). The measured characteristic impedance of the microstrip line was 42.87 Ω, providing a reference for validating the simulated TDR profile. Both the S-parameters and TDR curves were used to identify the HHSR value that best reproduced the real electrical behavior of the PCB across the tested frequency range.

RESULTS & DISCUSSION

Optimal Hall–Huray Surface Ratio
The parametric sweep showed that **HHSR = 9** produced the closest agreement between simulation and measurement.
At **10 GHz**, the difference in insertion loss (S21) between HFSS and the VNA was **below 0.04 dB**, indicating excellent alignment of conductor-loss modeling.

S-Parameter Comparison
The simulated and measured S21 curves follow the same trend across the entire frequency range, confirming that the dielectric and roughnes models accurately capture the PCB behavior.
For S11, the measured values reached approximately –22.8 dB, while simulations showed higher reflections (≈ –9.9 dB).
This mismatch is attributed to secondary factors not fully captured by the simulation, such as manufacturing tolerances, oxidation, connector transitions and small dielectric variations.

TDR and Impedance Analysis
The TDR results showed strong correlation:
•Measured impedance: 42.87 Ω
•Simulated impedance: 41.36 Ω

This ≈ 1 Ω difference indicates that the model closely reproduces the real characteristic impedance, validating the accuracy of the material and geometry assumptions.

Method Performance
Compared with traditional roughness-extraction techniques (profilometry, micrographs or pure numerical fitting), the proposed HFSS + VNA method provides:
•**High accuracy** with minimal laboratory requirements;
•**Moderate complexity**, suitable for design engineers;
•**Direct applicability** to real PCB stackups without destructive testing.
These results demonstrate that extracting HHSR through simulation–measurement matching is reliable, repeatable and practical for high-speed PCB design workflows.

CONCLUSION

The proposed method successfully extracted the **Hall–Huray Surface Ratio (HHSR)** by matching HFSS simulations with VNA/TDR measurements.
The optimal value (**HHSR = 9**) produced very close agreement with real PCB behavior, including **< 0.04 dB** insertion-loss difference at **10 GHz** and **≈1 Ω** TDR deviation.
This confirms the accuracy of the modeling approach and shows that the method is **practical, reliable, and easily applicable** to high-speed PCB design.

FUTURE WORK / REFERENCES

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3. Shlepnev, Y. Dielectric and Roughness Model Identification Using VNA Measurements, 2014.