An FPGA Platform Proposal for real-time Acoustic Event Detection: Optimum platform implementation for audio recognition with time restrictions

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1. Description of the problem

- Human activities monitoring has become a common issue
- Acoustic sensing using microphones is less intrusive than other common surveillance systems, as the use of cameras
- GTM is nowadays involved in two applications: SmartCity sensing (DYNAMAP Life LIFE ENV/IT/001254) and HomeSound (2014-SGR-0590), a home surveillance system for the elderly
- The acoustic signal processing has to be solved in a low cost hardware platform
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2. Goals of our paper are presented

- A study of the most suitable platform for acoustic event recognition taking into account
  - commercial platforms price
  - Computational complexity of the algorithms

- First approach to signal processing algorithms adaptation for the chosen platform
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3. Hardware platforms comparison

The comparison of the platforms has included the following microcontroller manufacturers:

- Renesas Technology
- Freescale Semiconductor
- ST Microelectronics
- Microchip Technology
- NXP Semiconductors
- Texas Instruments
- Infineon Technologies
3. Hardware platforms comparison

- **System requirements:**
  - 48 kHz of sampling frequency
  - an overlap of around 50% between frames
  - frames of 30 ms duration

- **The platform has to compute:**
  - the acquisition process
  - other signal processing algorithms
    - Windowing, FFT, 48 FIR filters (for feature extraction), DCT, etc.
  - manage the TCP/IP stack
3. Hardware platforms comparison

- The table shows the execution time for FFT and FIR algorithm for different number of points and different system frequency for a CORTEX-M3

- The proposal in this paper is the use of a low cost FPGA and its programmability paradigm, exploiting parallelization for real time applications
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4. HW proposal and algorithm implementation

- **Basis-3 Digilentinc Platform description**
  - MCB to manage auxiliary DDR memories
  - DCMs able to modify some aspects of the clock signals
    - Multiply or divide the input frequency
    - Condition a clock
    - Phase shift
    - Eliminate clock skew
    - Mirror, forward or rebuffer a clock signal
  - Block RAMs to implement two independent 18 kbits or one 36 kbits in Xilinx series 7 FPGA
  - A DSP block with pre-adder, multiplication and accumulator

<table>
<thead>
<tr>
<th>Basys-3</th>
<th>Slices</th>
<th>Logic Cells</th>
<th>Block RAM</th>
<th>DSPs</th>
<th>Price</th>
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</thead>
<tbody>
<tr>
<td>XC7A35T-1CPG236C</td>
<td>33280</td>
<td>33280</td>
<td>1800 kbit</td>
<td>90</td>
<td>150 $</td>
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</table>
4. HW proposal and algorithm implementation

- Algorithm implementation stages:
  - Windowing
  - FFT
  - 48 GTCC filter banks
  - Square root
  - Audio frames 30 ms long, results in 1440 samples at 48 ksp
4. HW proposal and algorithm implementation

- Implementation of windowing proposed to insert the data to the FFT block

![Diagram of the proposed hardware implementation](image-url)
4. HW proposal and algorithm implementation

- Resources from Basys-3 platform used by the presented implementations

<table>
<thead>
<tr>
<th>Basys-3</th>
<th>LUT</th>
<th>FF</th>
<th>BRAM</th>
<th>DSP</th>
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<td>FFT</td>
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<td>1385</td>
<td>4</td>
<td>4</td>
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<td>48 Filter Banks</td>
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<td>48</td>
<td>0</td>
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<tr>
<td>Square Root</td>
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<td>0</td>
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<td>Total</td>
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<td>24800</td>
<td>11</td>
<td>25</td>
</tr>
</tbody>
</table>
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5. Conclusions

- Basys-3 is a good trade-off between cost and features for audio detection algorithm implementation.
- It satisfies real-time performance for the typical required conditions.
- In future work we will implement a Microblaze in the FPGA in order to control the system remotely through Ethernet and to compute easily non-intensive parts of the algorithm.