LOW POWER PHASE LOCKED LOOP

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1. INTRODUCTION

- A PLL is used in all SOC devices, it has a negative feedback loop that controls the phase of the output signal with the input signal along with phase error.
- It mainly consists of four blocks called phase frequency detector, charge pump with low pass Filter, a voltage controlled oscillator and a frequency divider.

2. METHODOLOGY

- A PLL is designed using 90 nm CMOS technology node with 1.8V supply voltage.
- PLL design has power consumption as low as 194.26µW with better transient analysis and DC analysis in an analog-to-digital environment.
- The proposed PLL design provides the best solution for many applications where a PLL is required due to its high performance but has to be accommodated in less area and low power consumption than state-of-the-art methods.

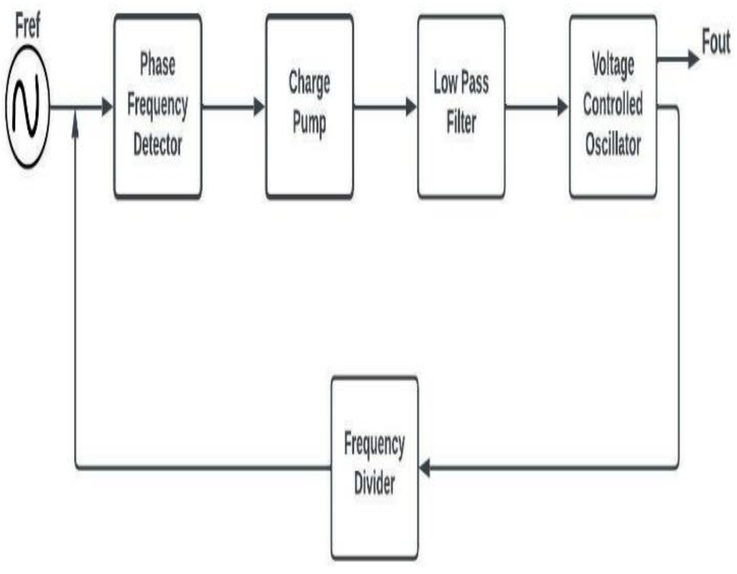

Fig 1. Block diagram of PLL

- Low power consumption, low area has been achieved by optimising the design of individual components of the PLL circuit.

3. DESIGN IMPLEMENTATION

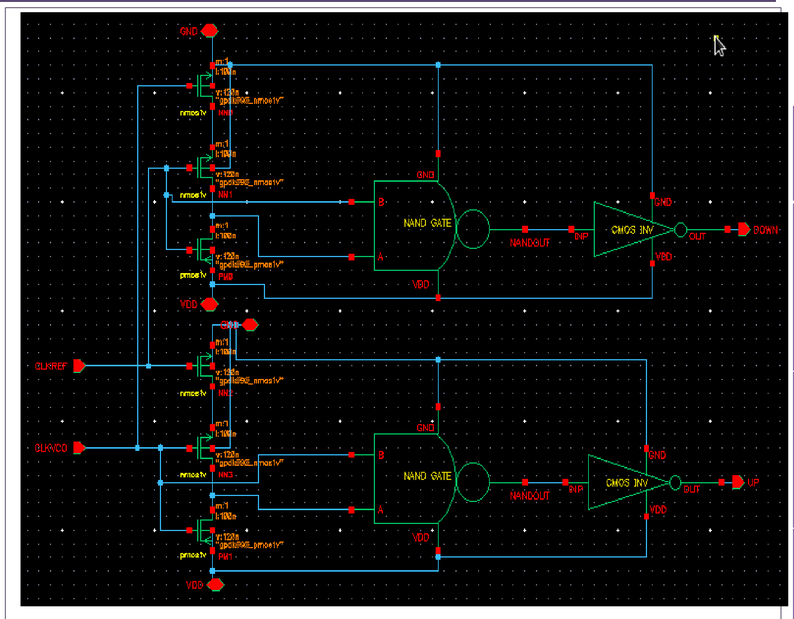

Fig 2. Schematic of Phase frequency detector

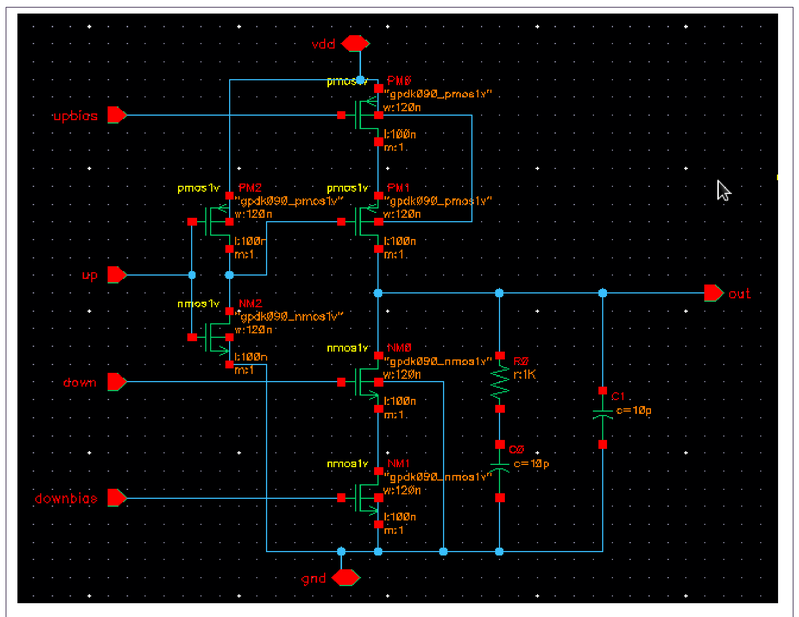

Fig 3. Charge pump with low pass filter

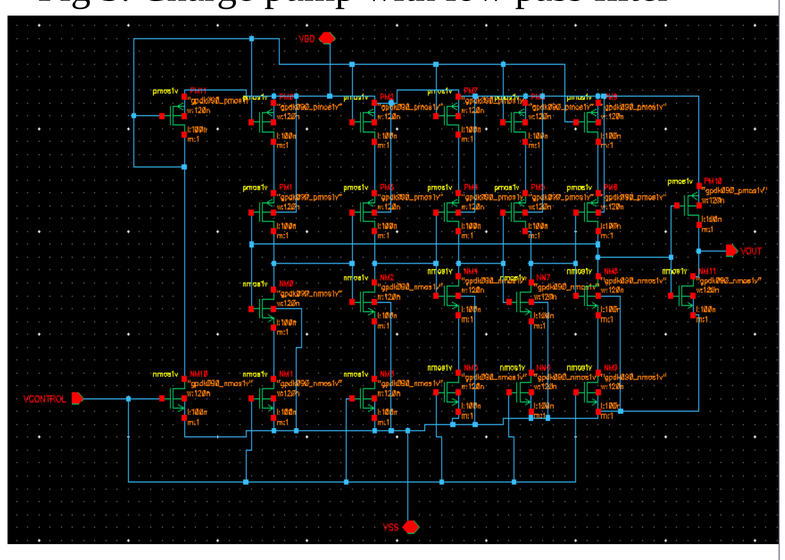

Fig 4. Schematic of voltage controlled oscillator

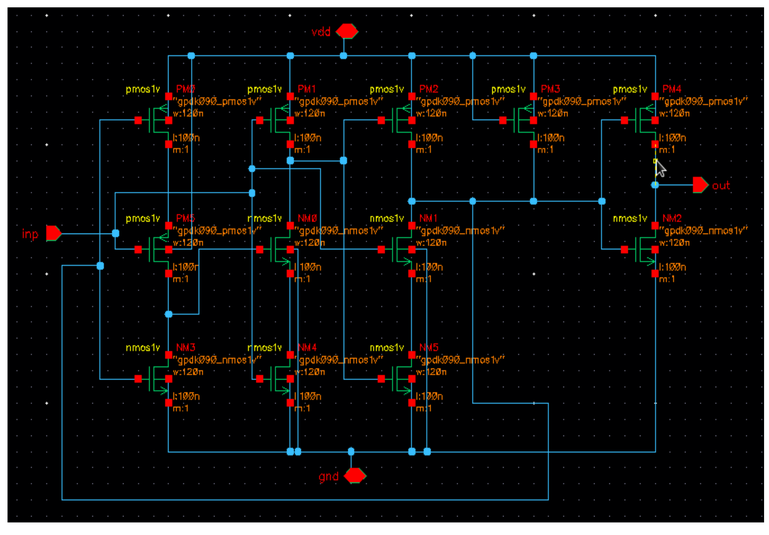

Fig 5. Schematic of frequency divider

5. COMPARISON BETWEEN PROPOSED AND EXISITNG PLL DESIGN

	Existing PLL	Proposed PLL
Number of transistors	56	48
Voltage supply	1.8 V	1.8 V
Operating frequency	1 GHz	1 GhHz
Power consumption	4.2mW	194.24 µW
Technology Node	90nm	90nm

6. CONCLUSION

- From the analysis the proposed PLL design has 14% decrease in number of transistors with reduced area and 1000 times less power consumption. So, the proposed PLL can be used effectively used in low power digital electronic applications and compact devices.

7. References

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