Verification of SoC using Advanced Verification Methodology

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INTRODUCTION

- ✓ In the past few decades, there has been tremendous progress in semiconductor industry from printed circuit boards to a multi-million gate design i.e., a System on Chip.
- ✓ SoC provides faster and reliable implementation design with low cost per gate and considerably low power consumption.
- ✓ In addition to this, it also offers a smaller physical size and with greater design security.
- ✓ The functional verification of the design is done by using system verilog and UVM testbench which includes creation of testcases, assertions and checkers for verifying different functionality as per the design specifications.
- ✓ A unique functional block which is present on the interconnect to slave interface is verified by using combination of checkers and test sequences.
- ✓ Trace monitoring of the transactions on AXI interface of the interconnect is done by programming different operational pointers and filters.

Challenges in verification

With devices getting smarter day by day, the complexity of operation shave gone up. Interaction points with users have increased. Some IoT based smart devices now continuously collect and process information.

- Reduction in available verification time
- Wrongly capturing specifications
- Usage scenarios for Devices
- Power consumption of devices
- Security
- Co-verification of hardware and software
- Analogue -digital amalgamation

Latest Trends in verification

- Simulation
- Mixed signal verification
- Verification and Power dependencies
- Data Analytics
- Checking inter-connectivity

Results

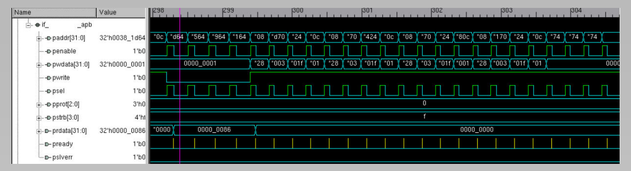


Figure 1: Configuration of Pointers

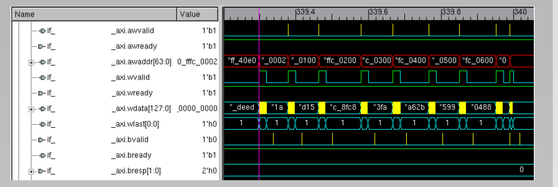


Figure 2: Write operation of AXI Burst Transfer

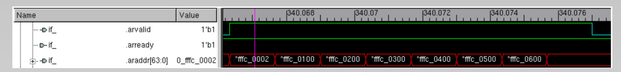


Figure 3: Read operation of AXI Burst Transfer

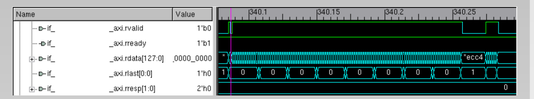


Figure 4: Read Response on AXI Burst Transfer

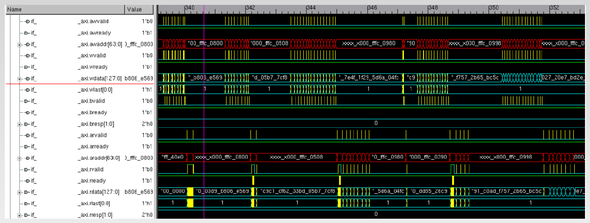


Figure 5: Burst Traffic on AXI Interface

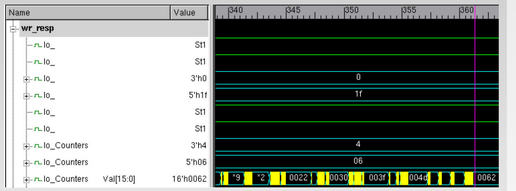


Figure 6: Write Request Transfers

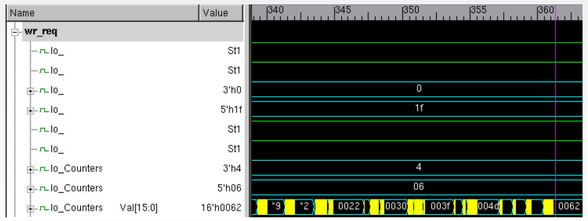


Figure 7: Write Response Transfers

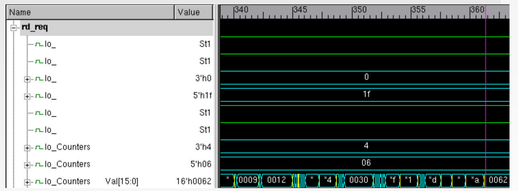


Figure 9: Read Request Transfers

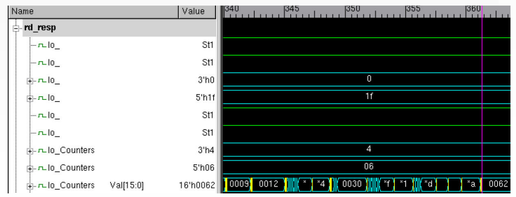
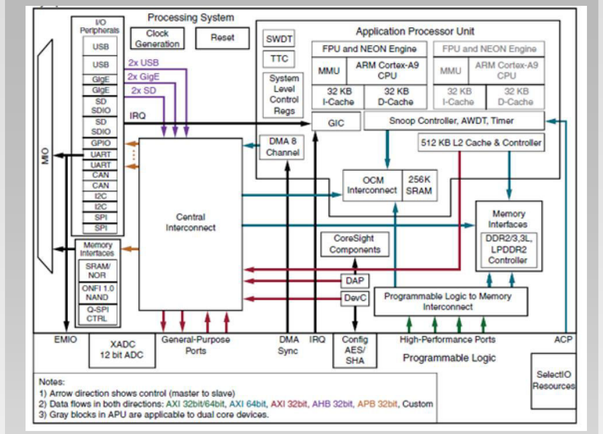


Figure 9: Read Response Transfers

SOC Architecture



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