ECP 2024 Conference

The 3rd International Electronic Conference on Processes

29–31 May 2024 | Online

NVPE: An FPGA Based Non-Volatile Processor Emulator for Intermittent Computing

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INTRODUCTION & AIM

Novel memory storage devices that occupy less physical area and are compatible with CMOS processes, such as resistive RAM [3], has led to the interesting study of non-volatile compute memories & devices. This development invites the opportunity for fully non-volatile Microprocessor (μP)s capable of rapid shutdown and startup.

This class of μP better enables intermittent computing systems applications. that wait until an energy-harvesting device has sufficient energy available before they do some useful work due to requiring less energy to power down safely.

Proper emulation of these systems will have a pivotal role in addressing potential design and implementation challenges in non-volatile processors.

METHOD

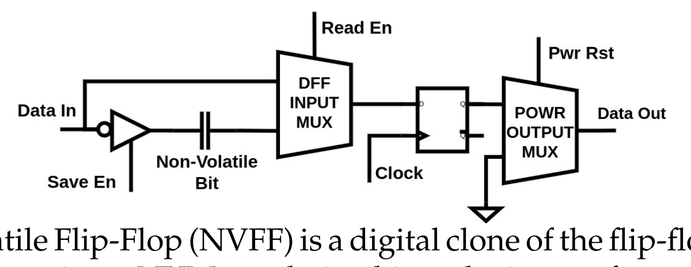


Figure (1) The Non-Volatile Flip-Flop (NVFF) is a digital clone of the flip-flop presented in [3]. It is realized by connecting a NVM emulation bit to the input of a standard flip-flop cell as well a multiplexer for the standard flip-flop input selection. Three signals: Save-En, Read-En, and Power-Rst simulate power-up/power-down scenarios

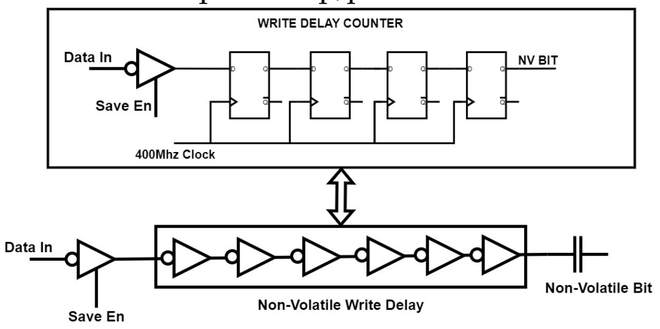


Figure (2) The NVFF incorporates two 4-bit counters that emulate variable read and write times for different non-volatile technologies..

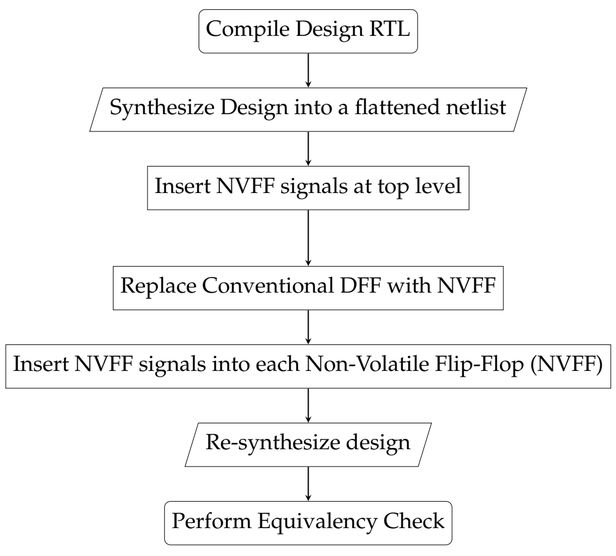


Figure (3) An automated cell replacement system (Non-Volatile Converter) which converts a conventional design into a non-volatile equivalent. The system follows the series of steps below to replicate the original design's functionality:

- First, the Converter uses Yosys [4], an open-source synthesis tool, to synthesize the Register-Transfer Level (RTL) design into a standard cell netlist.
- Following synthesis, the Converter adds the Save-En, Read-En, read-delay, write-delay, and Power-Rst to the netlist input/output ports.
- Next, the Converter parses the netlist in detail. During this parsing phase, each D Flip-Flop (DFF) cell within the netlist is replaced with our custom Non-Volatile Flip-Flop (NVFF).
- Last, the Converter adds the Save-En, Read-En, read-delay, write-delay, and Power-Rst to the input/output ports of each inserted NVFF

References

[1] *Advanced Encryption Standard*. 2020. URL: https://en.wikipedia.org/wiki/Advanced_Encryption_Standard.

[2] PERSISTLab. *Voltage traces*. https://github.com/PERSISTLab/BatterylessSim. 2023.

[3] Jean-Michel Portal et al. "Non-volatile flip-flop based on unipolar reram for power-down applications". In: *Journal of Low Power Electronics* 8.1 (2012), pp. 1–10. DOI: 10.1166/jolpe.2012.1172.

[4] Claire Wolf. *Yosys Open SYnthesis Suite*. https://yosyshq.net/yosys/.

RESULTS & DISCUSSION

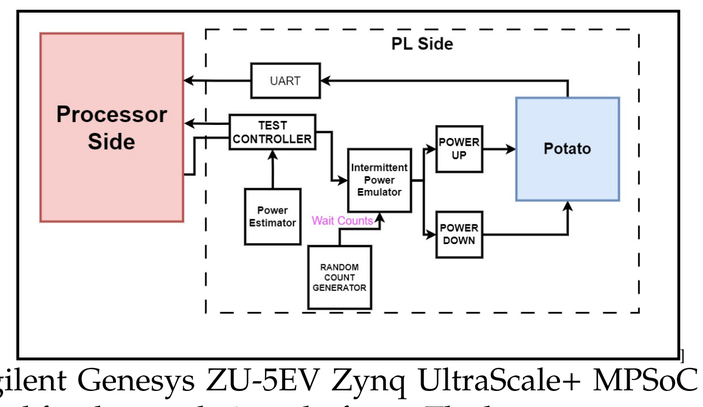


Figure (4) The Digilent Genesys ZU-5EV Zynq UltraScale+ MPSoC development board is utilized for the emulation platform. The host computer communicates through an Ethernet connection to the Linux operating system.

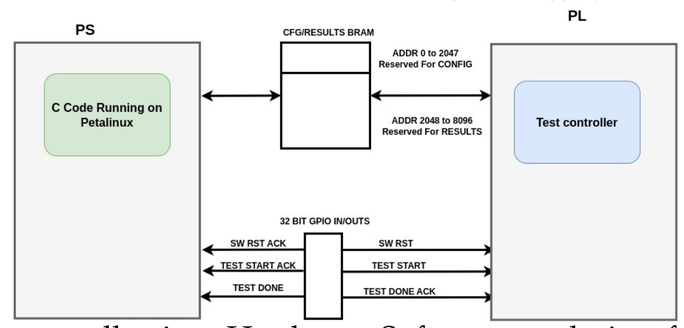
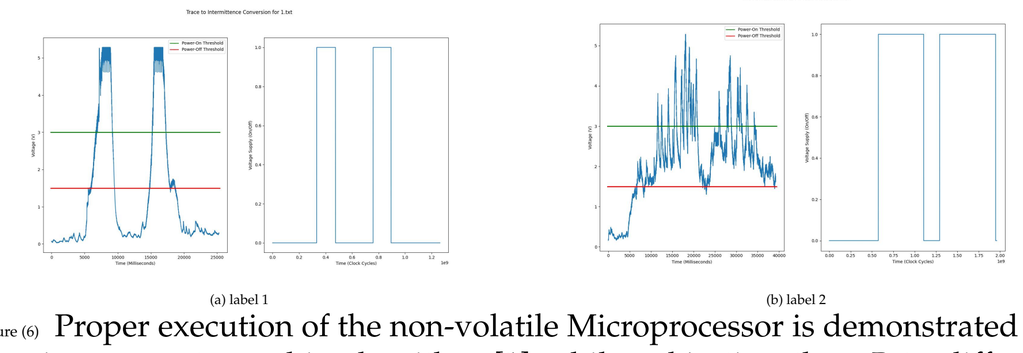


Figure (5) The test controller is a Hardware-Software co-design framework that oversees the actions of the NVP emulator.



(a) label 1 (b) label 2

Figure (6) Proper execution of the non-volatile Microprocessor is demonstrated by running a cryptographic algorithm [1] while subjecting the μP to different power signatures. The figures above show the trace to clock cycles conversion for traces in the PERSISTLab repository [2].

read delay (ns) \ write delay (ns)	0	2.5	5	7.5	10
0	pass	pass	pass	pass	fail
2.5	pass	pass	pass	pass	fail
5	pass	pass	pass	fail	fail
7.5	pass	pass	pass	fail	fail
10	fail	fail	fail	fail	fail

Table (1) We ran emulations with combinations of read and write delays up to 10 nanoseconds. Pass indicates that the NVP continues to compute and output the correct AES ciphertext on the UART peripheral while fail indicates that the NVP stops transmitting through UART peripheral or that the transmitted ciphertext is incorrect.

CONCLUSION

- Demonstrated that the NVPE is capable of simulating the variable read and write delay of the potential non-volatile flip-flops.
- Results highlight the importance of careful design for the power-up and power-down processes.
- NVPE is appropriate for verifying the behavior of non-volatile processor-based systems over long time frames, computing complex algorithms while mimicking the typical duty-cycling of energy intermittence systems

FUTURE WORK / REFERENCES

- Future work could utilize the NVPE in analyzing different combinations of non-volatile modules as part of a SOC centralized around the NVP.
- Subsequent work could analyze the states of the NVP in failed-restore situations and use the state values to develop countermeasures that identify and effectively act on failed-restore occurrences