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Exploring the Impact of Key Design Parameters on Double-Gate TFET Performance for Low-Power Applications

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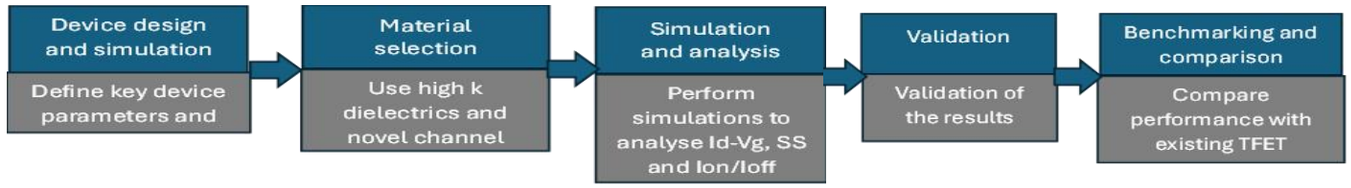
Abstract

This work compares DG-TFET and DG-MOSFET performance while optimizing TFET structure by varying silicon body thickness (5–15 nm) and high-k gate dielectrics. Owing to low SS, minimal leakage, and high ON current, DG-TFETs offer strong potential for low-power and biosensing applications. The optimized device achieves a 31.4 mV/dec subthreshold slope, 0.46 V threshold voltage, I_{off} of 2.68×10^{-16} A, and I_{on} of 5.91×10^{-5} A, with dielectric-dependent performance improvements.

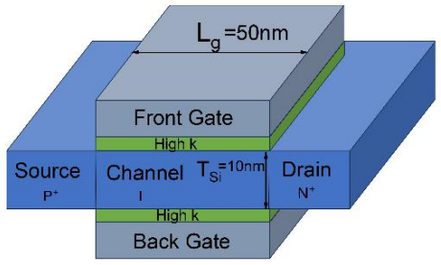
Introduction

As MOSFETs scale toward nanoscale limits, TFETs have emerged as promising alternatives due to their band-to-band tunneling–based operation, enabling SS < 60 mV/dec, very low leakage, and high ION/IOFF. Conventional TFETs, however, often suffer from low ON current. The DG-TFET designed in this work, incorporating a high-k dielectric and optimized silicon body thickness, achieves I_{on} = 59.1 µA, I_{off} = 2.68×10^{-16} A, I_{on} / I_{off} = 2.2×10^{11}, SS = 31.75 mV/dec, and V_{th} = 0.469 V, meeting ITRS 2015 low-power targets and making it suitable for biosensing. The study also analyzes interface trap charges, showing their significant influence on SS, ON current, and transconductance in DG-TFETs and DG-MOSFETs.

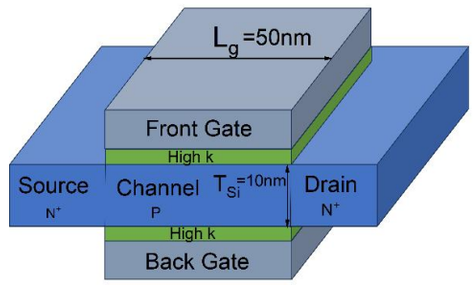
Methodology & Implementation

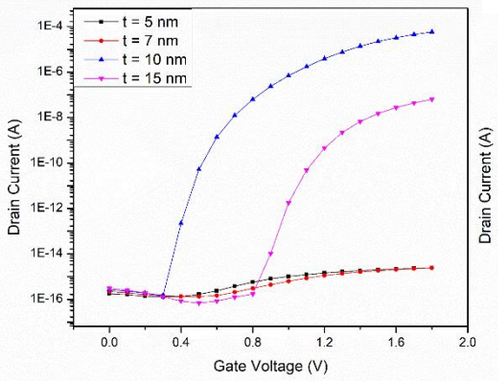


DG TFET

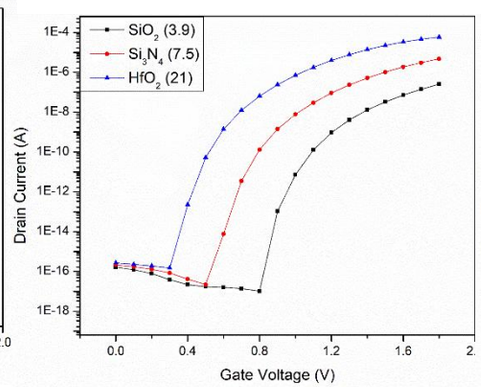


DG MOSFET

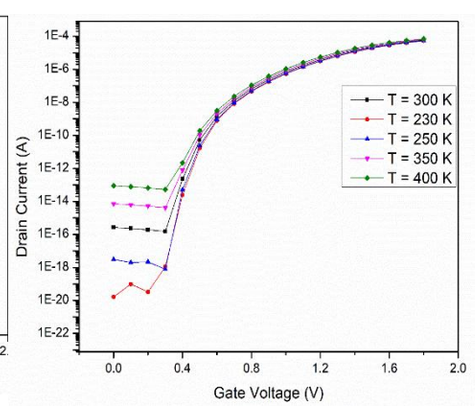




I_d-V_{gs} characteristics for various silicon body thicknesses



I_d-V_{gs} characteristics for various silicon body thicknesses



I_d-V_{gs} characteristics for various temperatures.

Device parameters used for design

Parameter	Value
Channel length (L_g)	50 nm
T_{si}	10 nm
T_{ox}	3 nm
Source length (L_s)	30 nm
Drain length (L_d)	30 nm
Source doping P+	1×10^{20} cm^{-3}
Drain doping N+	5×10^{18} cm^{-3}
Channel Doping	1×10^{17} cm^{-3}
HfO_2	21
SiO_2	3.9
Si_3N_4	7.5

Performance comparison of DGTFET and DGMOSFET

Device	SS (mV/dec)	V_t (V)	I_{OFF} (A)	I_{ON} (A/µm)	I_{ON}/I_{OFF}
DGMOSFET	61.1	0.36	1.97×10^{-8}	1.10×10^{-2}	5.5×10^{5}
DGTFET	31.4	0.46	2.68×10^{-16}	5.91×10^{-5}	2.2×10^{11}

Conclusion

This study demonstrates that the Double-Gate TFET (DGTFET) surpasses traditional DG-MOSFETs for low-power and high-sensitivity applications, particularly biosensing. The optimized DGTFET achieves a low subthreshold swing of 31.4 mV/dec and a high ION/IOFF ratio of 2.2×10^{11} by tuning silicon thickness, gate dielectric, and doping. High-κ dielectrics such as HfO_2 further enhance gate control, reduce leakage, and improve biomolecule-sensing capability. Silvaco Atlas simulations confirm stable performance under varying physical parameters and temperatures. The DGTFET emerges as an efficient, scalable, and thermally robust alternative to MOSFETs, offering superior switching behavior and sensitivity for next-generation nanoelectronic and biosensing technologies.

Future Works

Future work will focus on integrating advanced channel materials and experimentally validating biomolecule-specific sensing to further enhance DGTFET performance.

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