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RAMON LLULL UNIVERSITY

An FPGA Platform Proposal for real-time Acoustic Event Detection: Optimum platform implementation for audio recognition with time restrictions

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Index

1. Description of the problem
2. Goals of our paper are presented
3. Hardware platforms comparison
4. Hardware proposal and basic algorithm implementation
5. Conclusions

1. Description of the problem

- Human activities monitoring has become a common issue
- Acoustic sensing using microphones is less intrusive than other common surveillance systems, as the use of cameras
- GTM is nowadays involved in two applications: SmartCity sensing (DYNAMAP Life LIFE ENV/IT/001254) and HomeSound (2014-SGR-0590), a home surveillance system for the elderly
- The acoustic signal processing has to be solved in a low cost hardware platform

Index

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4. Hardware proposal and basic algorithm implementation
5. Conclusions

2. Goals of our paper are presented

- **A study of the most suitable platform for acoustic event recognition taking into account**
  - commercial platforms price
  - Computational complexity of the algorithms

- **First approach to signal processing algorithms adaptation for the chosen platform**

Index

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5. Conclusions

3. Hardware platforms comparison

- **The comparison of the platforms has included the following microcontroller manufacturers:**
  - Renesas Technology
  - Freescale Semiconductor
  - ST Microelectronics
  - Microchip Technology
  - NXP Semiconductors
  - Texas Instruments
  - Infineon Technologies

3. Hardware platforms comparison

- **System requirements:**
  - 48 kHz of sampling frequency
  - an overlap of around 50% between frames
  - frames of 30 ms duration

- **The platform has to compute:**
  - the acquisition process
  - other signal processing algorithms
    - Windowing, FFT, 48 FIR filters (for feature extraction), DCT, etc.
  - manage the TCP/IP stack

3. Hardware platforms comparison

FFT (ASM)	24 MHz Cycle count	24 MHz Time (μs)	48 MHz Cycle count	48 MHz Time (μs)	72 MHz Cycle count	72 MHz Time (μs)
FFT-64	3847	160	4025	84	4764	66
FFT-256	21039	876	22176	462	26065	362
FFT-1024	100180	4174	102057	2126	127318	1768
FIR-32	3516	146.5	3525	73.4	3727	5176

- **The table shows the execution time for FFT and FIR algorithm for different number of points and different system frequency for a CORTEX-M3**
- **The proposal in this paper is the use of a low cost FPGA and its programmability paradigm, exploiting parallelization for real time applications**

Index

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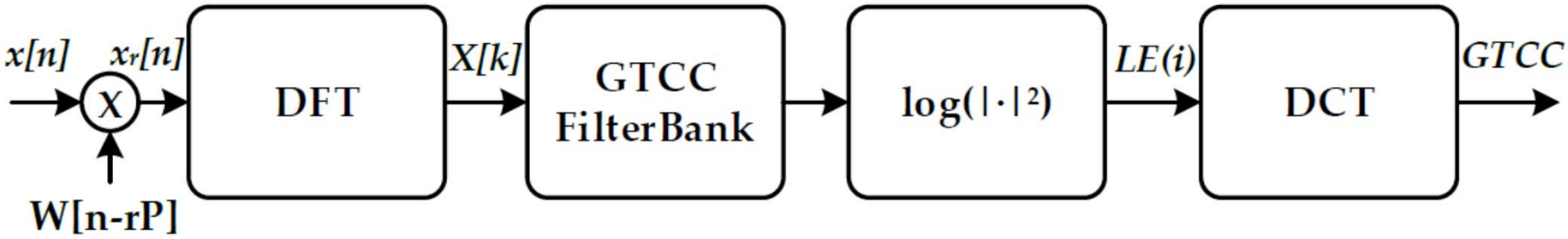
4. HW proposal and algorithm implementation

- **Basis-3 Digilentinc Platform description**
  - MCB to manage auxiliary DDR memories
  - DCMs able to modify some aspects of the clock signals
    - Multiply or divide the input frequency
    - Condition a clock
    - Phase shift
    - Eliminate clock skew
    - Mirror, forward or rebuffer a clock signal
  - Block RAMs to implement two independent 18 kbits or one 36 kbits in Xilinx series 7 FPGA
  - A DSP block with pre-adder, multiplication and accumulator

Basys-3	Slices	Logic Cells	Bloc RAM	DSPs	Price
XC7A35T-1CPG236C	33280	33280	1800 kbit	90	150 $

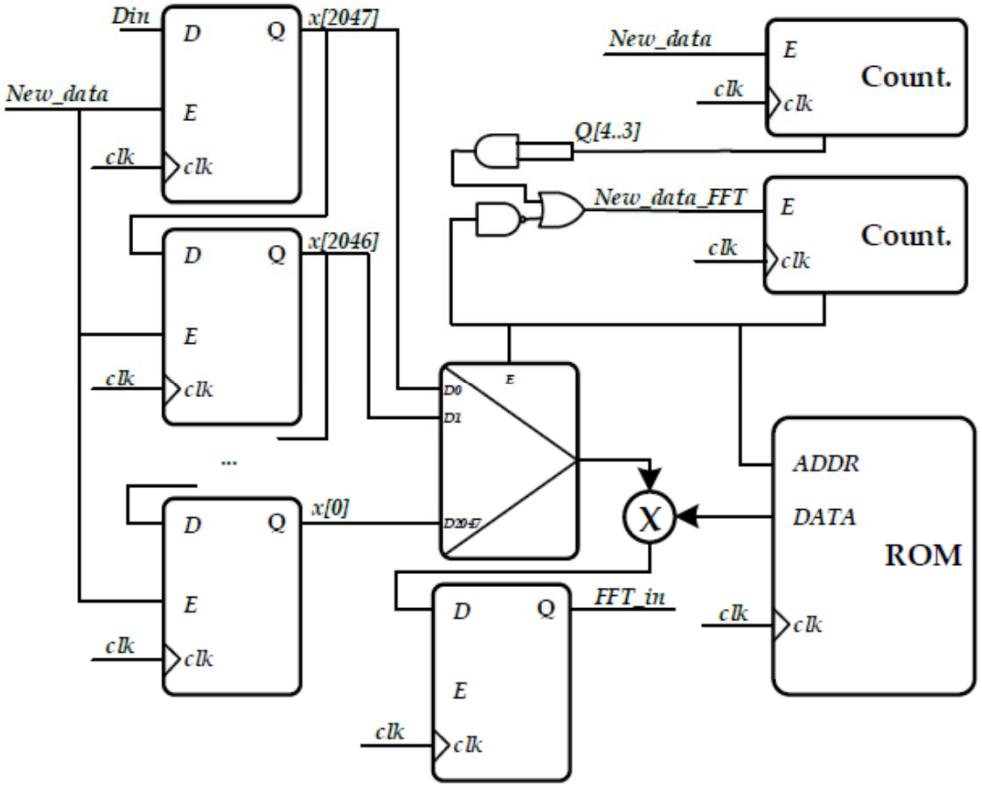
4. HW proposal and algorithm implementation

- **Algorithm implementation stages:**
  - Windowing
  - FFT
  - 48 GTCC filter banks
  - Square root
  - Audio frames 30 ms long, results in 1440 samples at 48 ksps



4. HW proposal and algorithm implementation

- **Implementation of windowing proposed to insert the data to the FFT block**



4. HW proposal and algorithm implementation

- **Resources from Basys-3 platform used by the presented implementations**

Basys-3	LUT	FF	BRAM	DSP
FFT	709	1385	4	4
48 Filter Banks	0	0	48	0
Square Root	783	0	0	0
Total	7949	24800	11	25

Index

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5. Conclusions

- Basys-3 is a good trade-off between cost and features for audio detection algorithm implementation
- It satisfies real-time performance for the typical required conditions
- In future work we will implement a Microblaze in the FPGA in order to control the system remotely through Ethernet and to compute easily non-intensive parts of the algorithm