Inverse Design of High Performance Silicon Photonic Devices

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Inverse design has triggered great research interests in integrated photonic design. It can be advantageous in discovering new photonic devices, because, unlike traditional device design (or forward design) where only a few parameters can be swept, a high-order multi-dimensional parameter space can be searched with an advance optimization algorithm for a global fitness that is often correlated with one or more performance metrics of the targeted device. Recently, such design concept has been applied to obtain ultra-compact photonic devices [1,2]. They, however, suffer greatly from performance degradation due to large out-of-plane scattering from strong scattering processes. In this talk, we utilize the concept of inverse design [1,2] and show that it is possible to design ultra-compact and highly performance silicon photonic devices that may have potential impact in future very large scale silicon photonic integrated circuits.

The first example of our inverse design is a waveguide crossing structure on silicon photonic platform with a footprint as small as ~ $1\times1um^2$, as shown in Fig. 1. In this design, the number of holes along with their sizes and positions and the size of the tapered crossing area are optimized with a customized Particle swarm optimization engine with the goal to maximize the average transmission efficiency in C-band. To our great surprise, multiple optimization instances yield the same design with three holes in each of the four waveguides forming a lens-like structure, suggesting the existence of a unique physical mechanism behind this design. As shown in Fig. 2, our simulation suggests that transmission efficiency more than 96% (corresponding to a insertion loss less than 0.16 dB), cross talk below -25 dB and back-reflection below -30 dB within the C-band operation can be achieved. Note that the reflection spectrum contains a relative sharp dip, a clear indication of a cavity resonance. Detailed analysis reveals that the working principle of our designed device is based on optical tunneling through a cavity formed at the waveguide crossing with 4 lens-like structures, which is a completely different physical mechanism from all the other reported ones used in making high efficient waveguide crossings. Our device was recently fabricated using electron beam lithography, followed by inductively coupled plasma etching. A top view SEM image of a typical device is shown in Fig 2. Notice that the three tiny holes (with diameters < 50 nm) are replaced intentionally with a lens to overcome fabrication difficulties. Our preliminary test shows that our fabrication device has an insertion loss less than 0.2 dB at 1550nm. Detailed tests are being conducted and comprehensive results will be presented at the talk.

Next, using the same design principle, I also would like to present a few other silico integrated devices also optimized for compact footprint and high efficiency. For example, an in-line high efficient mode converter between the fundamental quasi-TE mode and the first-order quasi-TE mode can be faithfully designed with a length less than 2.5 um. The conversion mechanism behind this ultra-compact is also revealed to be unique in this case.

In short, through this talk with a few important device examples, I would like to demonstrate that inverse design when used properly can be very powerful in discovering new mechanisms for photonic devices and in reducing device footprints.

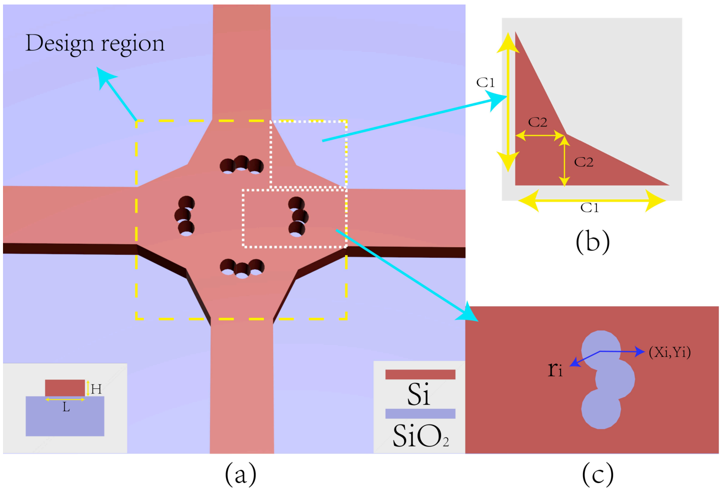

Fig. 1 (a) Schematic of our proposed waveguide crossing structure with etched holes (b) a zoom-in view of one tapered section at the corner of the two crossing waveguides, and (c) a zoom-in view of the etched holes.

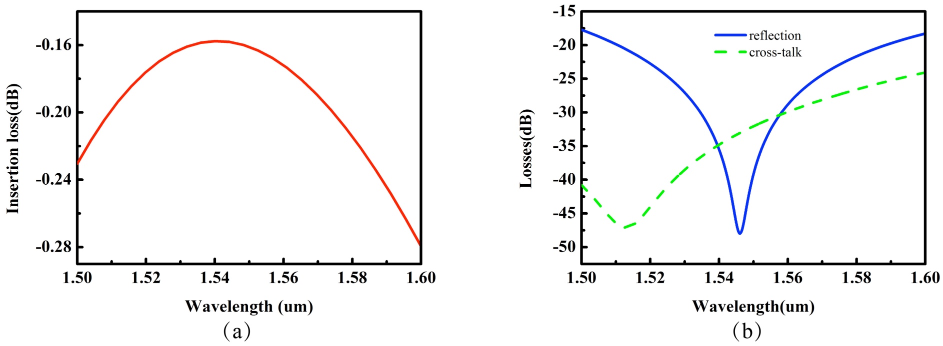

Fig. 2 Performance characteristics for the optimized waveguide crossing structure. (a) Insertion loss spectrum, and (b) reflection and cross-talk spectrum.

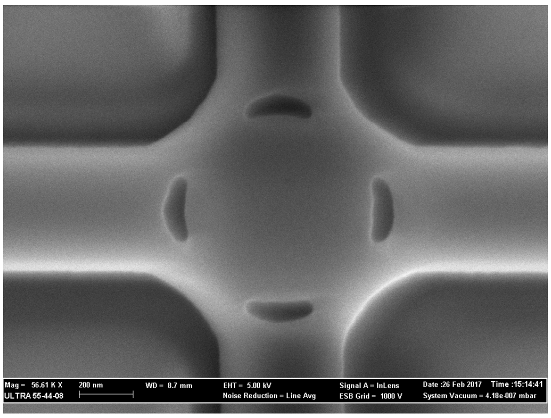

Fig. 3 SEM images of the fabricated waveguide crossing fabricated on a 220-nm-thick SOI device layer. A lens replaces the three holes in Fig. 1.

REFERENCES:

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