proceedings

MDPI

Proceedings

Temperature Dependence of Germanium Arsenide Field-Effect Transistors Electrical Properties †

Alessandro Grillo [1,2,*], Enver Faella [1], Filippo Giubileo [2], Aniello Pelella [1,2], Francesca Urban [1,2] and Antonio Di Bartolomeo [1,2,*]

[1] Physics Department "E. R. Caianiello", University of Salerno, Via Giovanni Paolo II 132, 84084 Fisciano, Salerno, Italy; efaella@unisa.it (E.F.); apelella@unisa.it (A.P.); furban@unisa.it (F.U.)
[2] CNR-SPIN Salerno Via Giovanni Paolo II 132, 84084 Fisciano, Salerno, Italy; filippo.giubileo@spin.cnr.it
* Correspondence: agrillo@unisa.it (A.G.); adibartolomeo@unisa.it (A.D.B.)
† Presented at the 2nd International Online-Conference on Nanomaterials, 15–30 November 2020; Available online: https://iocn2020.sciforum.net/.

Published: 15 November 2020

Abstract: In this work, we report the fabrication of germanium arsenide ($GeAs$) field-effect transistors with ultrathin channel and their electrical characterizations in a wide temperature range, from $20\,K$ to $280\,K$. We show that at lower temperatures the electrical conduction of the $GeAs$ channel is dominated by the 3D variable range hopping but becomes band-type at higher temperatures, after the formation of a highly conducting two-dimensional (2D) channel. The presence of this 2D channel, limited to few interfacial $GeAs$ layers, is confirmed by the observation of an unexpected peak in the temperature dependence of the carrier density per area at $\sim 75\,K$. Such a feature is explained considering a model based on a temperature-dependent channel thickness, corroborated by numerical simulations, that show excellent agreement with the experimental data.

Keywords: germanium arsenide; 2D conduction; field-effect transistors; carrier concentration; variable range hopping

1. Introduction

Recent interest in research on two-dimensional (2D) materials has led to the exploration of new classes of layered materials beyond graphene and transition metal dichalcogenides. Among these, the binary compounds of groups IV and V are assuming considerable importance since theoretical studies have proved their crystalline layered structures with orthorhombic ($Cmc2_1$ for SiP and $Pbam$ for SiP_2 and $GeAs_2$) or monoclinic ($C2/m$ for GeP, $GeAs$, and $SiAs$) symmetries [1–4]. Particularly, $GeAs$ has been considered for possible optoelectronic applications and for its high in-plane anisotropy [5,6]. Figure 1a shows the $GeAs$ crystal layered structure, in which each Ge atom is bonded to one Ge atom and three As atoms forming distorted $As_6@Ge_2$ octahedra [7]. Similar to TMDs, the $GeAs$ bandgap changes according to the number of layers. Numerical calculations and optical bandgap measurements, indicate that germanium arsenide indirect bandgap ranges from $\sim 0.57 - 0.65\,eV$ for the bulk [8,9] to $1.6 - 2.1\,eV$ for the monolayer [10,11].

In this work, we report the fabrication of $12\,nm$ thick $GeAs$ back-gate field effect transistors through mechanical exfoliation and their electrical characterization in a four-probe configuration and in a range of temperatures from $20\,K$ to $280\,K$. We find that at low temperature the conduction is dominated by 3D variable range hopping but becomes band-type at higher temperatures. This change in the conduction mechanism is due to the formation of a highly conducting 2D channel close to the gate, confirmed by the observation of an unexpected peak in the temperature dependence of

the carrier density per area at $\sim 75\ K$. The model is corroborated by numerical simulations that show an excellent agreement with the experimental data.

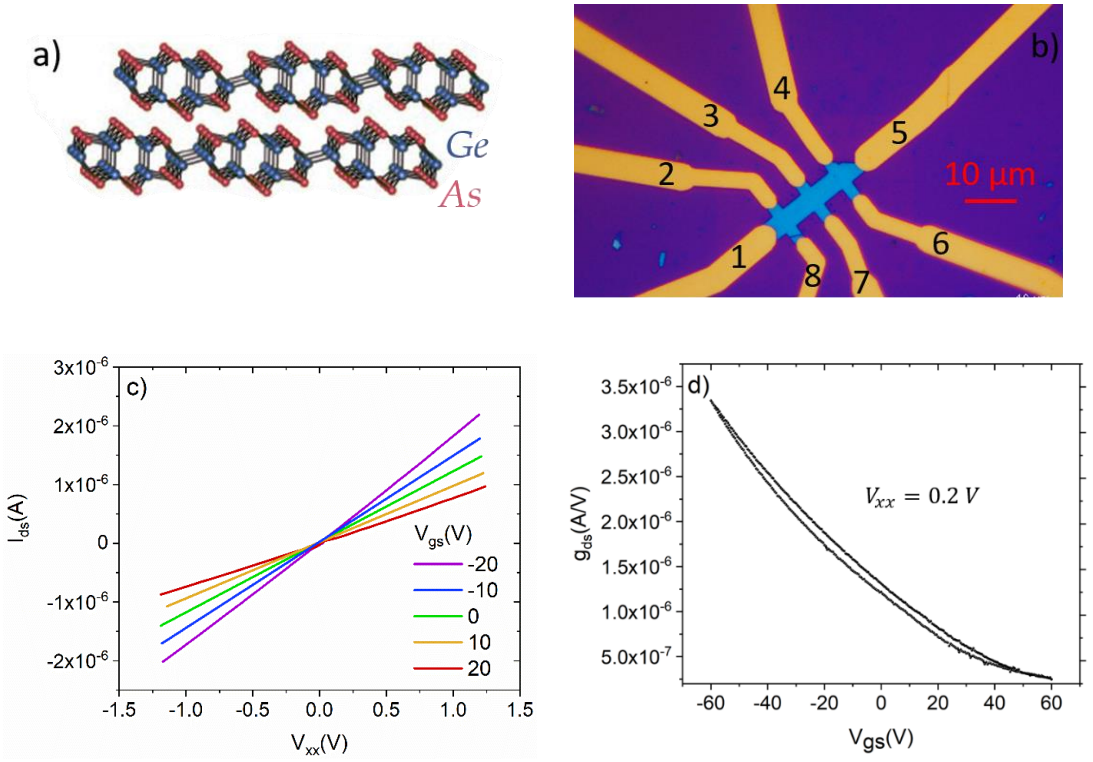


Figure 1. (**a**) Atom arrangement in $GeAs$ layers. (**b**) Optical image of the Hall bar device with Ni/Au electrodes. (**c**) Output characteristic recorded in four-probe configuration with V_{gs} bias between −20 V and 20 V. (**d**) Transfer characteristic recorded in four-probe configuration showed both on linear and logarithmic scale.

2. Results and Discussion

Figure 1b shows an optical image of a $12\ nm$ thick $GeAs$ flakes covered with eight $5\ nm\ Ni/40\ nm\ Au$ electrodes. Ultrathin $GeAs$ flakes were exfoliated from bulk $GeAs$ single crystals using a standard mechanical exfoliation method by adhesive tape. The flakes were transferred onto degenerately doped p-type silicon substrates, covered by $300\ nm$-thick SiO_2. Electron-beam lithography were performed on selected flakes to obtain a Hall bar structure. Finally, electron-beam evaporation was used to deposit the metal electrodes [12].

Contacts 1 to 4 were used to perform a standard four probe electrical characterization in which the current (I_{ds}) is measured between the outers contact (1 and 4) and the voltage drop (V_{xx}) is measured between the inner contacts (2 and 3).

Figure 1c shows the output characteristic i.e., the drain-source current as a function of the voltage drop between two inner contacts with the gate-source voltage (V_{gs}) as control parameter. It shows a linear behaviour that is not influenced by the gate potential which only changes the total conductance of the device. Moreover, it testifies the formation of ohmic contacts due to the alignment between the Ni Fermi level (work function $5.15\ eV$) below the valence band of $GeAs$. Figure 1d reports the transfer characteristic, i.e., the $g_{ds} - V_{gs}$ curve ($g_{ds} = I_{ds}/V_{xx}$ is the channel conductance) measured over a loop of the gate voltage. It shows a typical p-type behaviour mainly due to the presence of intrinsic defects such as Ge vacancies, the interaction with the SiO_2 gate dielectric and the oxidation of the topmost layers of the flake that would act as p-type dopants in the material and provide intragap states [1,2].

Figure 2a,b show the temperature dependence of the electric behaviour of the device in the $20 - 280\ K$ temperature range. Particularly, from Figure 2a we find that the conductance decreases lowering the temperature without any other apparent change in the behaviour of the device and from

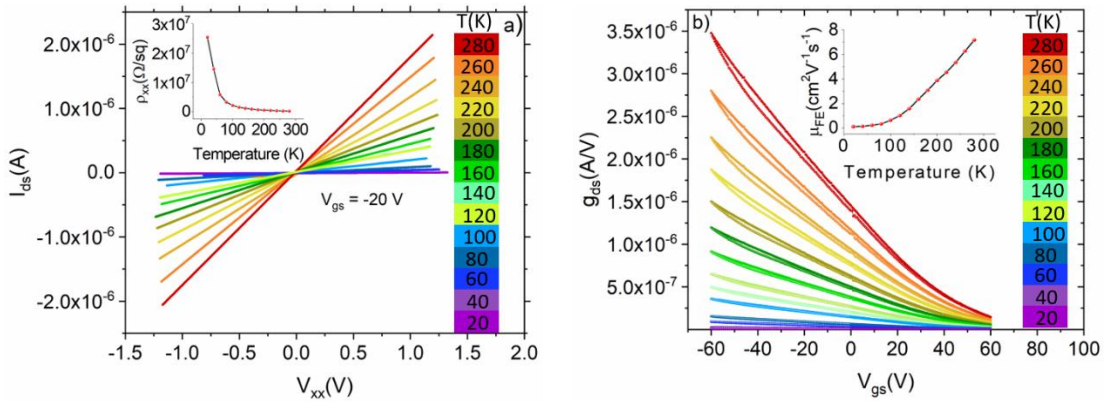
a linear fit of the $I_{ds} - V_{xx}$ curves recorded at $V_{gs} = -20V$, we estimate the resistivity ρ of the sample as a function of the temperature ($\rho = RW/L$, where R is the resistance evaluated from the fit and $L = 6\,\mu m$ and $W = 2.7\,\mu m$ are the channel length and width, respectively). The results of the fit are shown in the insect of Figure 2a in which a clear semiconductive behaviour is observed. Figure 2b reports the transfer characteristic of the device in which we defined the FET channel conductance as:

$$g_{ds} = \frac{I_{ds}}{V_{xx}} = \left(\frac{W}{L}\right) \mu_{FE}\, C_{ox}\, |V_{gs} - V_{th}\,|^{\alpha} \tag{1}$$

where μ_{FE} is the field-effect mobility, $C_{ox} = \epsilon_0 \cdot \frac{\epsilon_{SiO_2}}{t_{SiO_2}} = 1.15 \cdot 10^{-8}\, F/cm^2$ is the capacitance per unit area of the gate dielectric, where $\epsilon_0 = 8.85 \cdot 10^{-14}\, F/cm^2$, $\epsilon_{SiO_2} = 3.9$ and $t_{SiO_2} = 300\,nm$ are the vacuum permittivity, the SiO_2 relative permittivity and thickness, respectively, V_{th} is the threshold voltage and $\alpha \geq 1$ is a dimensionless parameter which accounts for a possible V_{gs}-dependence of the mobility [13]. In order to have a fair comparison with the values of ρ obtained from $g_{ds} - V_{xx}$ curves at $V_{gs} = -20\,V$, we performed linear fit of the transfer characteristics in a small interval around $V_{gs} = -20\,V$ in which we can consider $\alpha = 1$. From the fit we can extrapolate the mobility at each temperature as shown in the insect of Figure 2b. We find a quadratic dependence, $\mu_{FE} \sim T^2$, pointing towards a mobility dominated by Coulomb scattering due to ionized impurities [14]. A deeper analysis of the ρ versus T graph, shown in the insect of Figure 2a, reveals that the electrical conduction follows two different mechanisms at low and high temperature, respectively. Indeed, we notice that the best fitting of the experimental data at low temperature is obtained using the variable range hopping conduction (VRH). According to VRH theory the relation between ρ and T can be expressed as [15]:

$$\rho(T) = \rho_0\, exp\left(\frac{T_0}{T}\right)^{\frac{1}{n+1}} \tag{2}$$

where ρ_0 depends on the square root of T, T_0 is a constant and n indicates the dimensionality of the system [16].



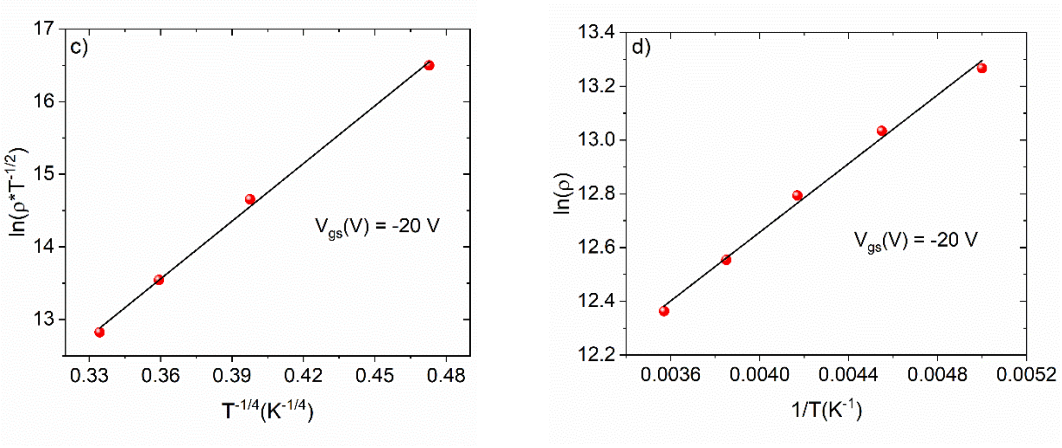


Figure 2. (**a**) I_{ds} versus V_{xx} curves at different temperatures. The insect shows the channel resistivity as function of the temperature. (**b**) Transfer characteristics recorded for a loop of the voltage bias at different temperatures. The insect shows the field effect mobility as function of the temperature (**c**) Experimental data and linear fit of $ln\,(\rho * T^{-\frac{1}{2}})$ at $V_{gs} = -20\,V$ as function of $T^{-\frac{1}{4}}$ at low temperature indicating the three-dimensional nature of the investigated system. d) Experimental data and linear fit of $ln(\rho)$ at $V_{gs} = -20\,V$ as function of T^{-1} at high temperature indicating the band conduction regime of the investigated system.

Figures 2c shows $\ln\,(\rho * T^{-\frac{1}{2}})$ as function of $T^{-\frac{1}{4}}$ in the range $20\,K$ to $80\,K$. The linearity demonstrates that the conduction is bulk type (3D) for $T < 80\,K$, i.e., it occurs through the entire flake constituted of ~ 20 atomic layers. Figure 2d shows the trend for $T > 180\,K$. We observe an exponential increase with the inverse of temperature that indicates that the thermal excitation of carriers (holes) to the valence band leads to a band conduction regime, $\rho \propto exp(E_A/kT)$, as expected after the formation of a highly conductive 2D channel in the $GeAs$ transitor.

In order to try to explain this strange passage from a bulk to a 2D conduction we calculate the carrier density per unit area n (in cm^{-2}) as a function of the temperature. Indeed, having computed $\mu_{FE}\,(T)$ and $\rho(T)$ at each of the considered temperatures, n can be obtained from the relation:

$$n(T) = 1/(q\rho(T)\mu_{FE}\,(T)) \tag{3}$$

where q is the electron charge. Figure 3a shows that $n(T)$ exhibits an unexpected and pronounced peak at $T{\sim}75\,K$, followed by a smoother increase for $T > 150\,K$. In a doped three-dimensional semiconductor, the carrier density would show a different temperature behaviour [14]. Specifically, an initial rapid increase due to the ionization of dopant atoms by thermal energy (freeze-out region, up to $\sim 150\,K$ for medium-doped Si) would be followed by a plateau over a wide temperature range when complete ionization is reached (extrinsic region, $\sim 150 - 500\,K$ for medium-doped Si), and would finally evolve in an exponential increase at higher temperatures due to intrinsic generation of electron-hole pairs (intrinsic region). To explain both the reported anomalous behaviour and the modification from a bulk to a 2D conduction due to increasing temperature, we propose a model that considers a temperature dependent thickness of the channel in which most of the conduction occurs. Indeed, we notice that the 2D carrier density per unit area can be expressed as $n(T) = \varphi(T)\tau(T)$ where φ is the carrier density per unit volume in cm^{-3} and τ is the thickness of the conducting channel. The current in the $GeAs$ flake is due to carriers injected from the Ni contacts that overcome a potential barrier, E_A, between the contacts and the channel region. Therefore, $\varphi(T)$ in the region between the inner contacts can be expressed as [17]:

$$\varphi(T) = A\,exp[-E_A/kT] \tag{4}$$

where k is the Boltzmann constant and A is a proportionality constant that can be considered as a fitting parameter of the model.

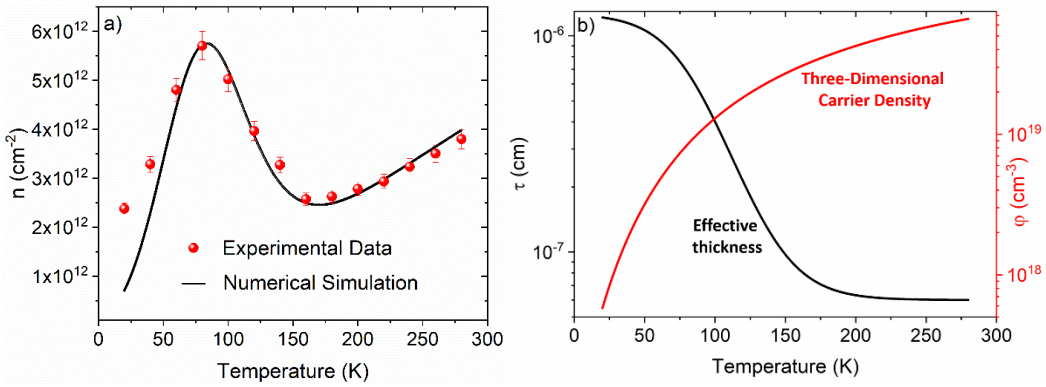


Figure 3. (**a**) Numerical simulation of the 2D carrier density as function of the temperature for $V_{gs} = -20\ V$ superimposed to the experimental data (red dots). (**b**) Effective thickness of the channel (black line) and three-dimensional carrier density (red line) as function of the temperature for $V_{gs} = -20\ V$

At low temperature ($< 80\ K$), there is a limited amount of carriers as well as high intralayer resistance that suppresses the vertical transport with respect to the in-plane one [18,19]. In this regime, conduction occurs mainly through the layers in closer contact with the metal leads (especially the topmost ones) and the gate electric field controls the entire flake thickness. With raising temperature, defect ionization and injection from the contacts increase. The new available carriers, pushed by the applied gate voltage and the favourable vertical band bending toward the interface with the gate dielectric, form a 2D channel, which becomes more and more conductive with the rising temperature. This channel now screens the gate field, and any variation of the gate voltage affects mainly the bottommost layers of the flake. In this regime, the conduction is dominated by few atomic $GeAs$ layers closer to the gate, i.e., the effective conducting thickness $\tau(T)$ controlled by the gate is reduced.

To test the model, with an appropriate choice of $\varphi(T)$ and $\tau(T)$, we computed $n(T)$ obtaining an excellent agreement with the experimental data, as shown in Figure 3a, where we display $n(T)$ at $V_{gs} = -20\ V$. The carrier density per volume $\varphi(T)$, given by Equation (4), is shown by the red line of Figure 3b, with E_A obtained as fitting parameter. For $\tau(T)$, we used a step-like function, $\tau(T) = A/(1 + exp(B * T)) + C$, represented by the black curve shown in Figure 3b, in which A is the initial thickness of the whole flake, i.e., $\sim 12\ nm$, C is the thickness of a single $GeAs$ layer ($0.6\ nm$), and B is a fitting parameter used to simulate a smooth transition in the $70 - 150\ K$ range. Finally, the model is further corroborated by the estimation of the Debye screening length $L_D = \sqrt{\frac{\epsilon\epsilon_0 kT}{q^2\varphi}}$, that gives the length over which the electric field strength drops by a factor $1/e$ (here $\epsilon = 8$ is the dielectric constant at room temperature of the material [20]). From our data, we estimate $L_D \sim 0.4\ nm$ at room temperature, confirming that the gate electric field is substantially screened in the layer closer to the gate.

3. Conclusions

We fabricated back-gate field effect transistors with ultrathin $GeAs$ films and investigated their electrical properties over a wide temperature range, from $20\ K$ to $280\ K$. We found a p-type behaviour with temperature increasing conductivity. We find that the conduction is dominated by the 3D variable range hopping at lower temperatures but becomes band-type at higher temperatures, when a highly conducting 2D channel is formed. We observed that the carrier density in $GeAs$ flakes depends on temperature with a pronounced and broad peak around $75\ K$. We proposed a model based on a temperature-dependent channel thickness to explain such an anomaly that shows an excellent agreement with the experimental data.

References

1. Wu, P.; Huang, M. Stability, bonding, and electronic properties of silicon and germanium arsenides: Stability, bonding, and electronic properties of Si and Ge arsenides. *Phys. Status Solidi (b)* **2016**, *253*, 862–867, doi:10.1002/pssb.201552598.
2. Jung, C.S.; Kim, D.; Cha, S.; Myung, Y.; Shojaei, F.; Abbas, H.G.; Lee, J.A.; Cha, E.H.; Park, J.; Kang, H.S. Two-dimensional GeAs with a visible range band gap. *J. Mater. Chem. A* **2018**, *6*, 9089–9098, doi:10.1039/C8TA02676A.
3. Cheng, A.-Q.; He, Z.; Zhao, J.; Zeng, H.; Chen, R.-S. Monolayered Silicon and Germanium Monopnictide Semiconductors: Excellent Stability, High Absorbance, and Strain Engineering of Electronic Properties. *ACS Appl. Mater. Interfaces* **2018**, *10*, 5133–5139, doi:10.1021/acsami.7b17560.
4. Shojaei, F.; Kang, H.S. Electronic Structures and Li-Diffusion Properties of Group IV–V Layered Materials: Hexagonal Germanium Phosphide and Germanium Arsenide. *J. Phys. Chem. C* **2016**, *120*, 23842–23850, doi:10.1021/acs.jpcc.6b07903.
5. Guo, J.; Liu, Y.; Ma, Y.; Zhu, E.; Lee, S.; Lu, Z.; Zhao, Z.; Xu, C.; Lee, S.-J.; Wu, H.; et al. Few-Layer GeAs Field-Effect Transistors and Infrared Photodetectors. *Adv. Mater.* **2018**, *30*, 1705934, doi:10.1002/adma.201705934.
6. Yang, S.; Yang, Y.; Wu, M.; Hu, C.; Shen, W.; Gong, Y.; Huang, L.; Jiang, C.; Zhang, Y.; Ajayan, P.M. Highly In-Plane Optical and Electrical Anisotropy of 2D Germanium Arsenide. *Adv. Funct. Mater.* **2018**, *28*, 1707379, doi:10.1002/adfm.201707379.
7. Blachnik, R.; Irle, E. Das System Gallium-Tellur. *J. Less Common Met.* **1985**, *113*, L1–L3, doi:10.1016/0022-5088(85)90158-4.
8. Lee, K.; Kamali, S.; Ericsson, T.; Bellard, M.; Kovnir, K. GeAs: Highly Anisotropic van der Waals Thermoelectric Material. *Chem. Mater.* **2016**, *28*, 2776–2785, doi:10.1021/acs.chemmater.6b00567.
9. Rau, J.W.; Kannewurf, C.R. Optical Absorption, Reflectivity, and Electrical Conductivity in GeAs and Ge As 2. *Phys. Rev. B* **1971**, *3*, 2581–2587, doi:10.1103/PhysRevB.3.2581.
10. Zhou, L.; Guo, Y.; Zhao, J. GeAs and SiAs monolayers: Novel 2D semiconductors with suitable band structures. *Phys. E Low-Dimens. Syst. Nanostructures* **2018**, *95*, 149–153, doi:10.1016/j.physe.2017.08.016.
11. Mortazavi, B.; Shahrokhi, M.; Cuniberti, G.; Zhuang, X. Two-Dimensional SiP, SiAs, GeP and GeAs as Promising Candidates for Photocatalytic Applications. *Coatings* **2019**, *9*, 522, doi:10.3390/coatings9080522.
12. Grillo, A.; Di Bartolomeo, A.; Urban, F.; Passacantando, M.; Caridad, J.M.; Sun, J.; Camilli, L. Observation of 2D Conduction in Ultrathin Germanium Arsenide Field-Effect Transistors. *ACS Appl. Mater. Interfaces* **2020**, *12*, 12998–13004, doi:10.1021/acsami.0c00348.
13. Di Bartolomeo, A.; Genovese, L.; Giubileo, F.; Iemmo, L.; Luongo, G.; Foller, T.; Schleberger, M. Hysteresis in the transfer characteristics of MoS 2 transistors. *2D Mater.* **2017**, *5*, 015014, doi:10.1088/2053-1583/aa91a7.
14. Sze, S.M.; Ng, K.K. *Physics of Semiconductor Devices*, 3rd ed.; Wiley-Interscience: Hoboken, NJ, USA, 2007; ISBN 978-0-471-14323-9.
15. Mott, N.F. Conduction in glasses containing transition metal ions. *J. Non-Cryst. Solids* **1968**, *1*, 1–17, doi:10.1016/0022-3093(68)90002-1.
16. Barreteau, C.; Michon, B.; Besnard, C.; Giannini, E. High-pressure melt growth and transport properties of SiP, SiAs, GeP, and GeAs 2D layered semiconductors. *J. Cryst. Growth* **2016**, *443*, 75–80, doi:10.1016/j.jcrysgro.2016.03.019.
17. Ang, Y.S.; Yang, H.Y.; Ang, L.K. Universal Scaling Laws in Schottky Heterostructures Based on Two-Dimensional Materials. *Phys. Rev. Lett.* **2018**, *121*, 056802, doi:10.1103/PhysRevLett.121.056802.
18. Liu, Y.; Guo, J.; He, Q.; Wu, H.; Cheng, H.-C.; Ding, M.; Shakir, I.; Gambin, V.; Huang, Y.; Duan, X. Vertical Charge Transport and Negative Transconductance in Multilayer Molybdenum Disulfides. *Nano Lett.* **2017**, *17*, 5495–5501, doi:10.1021/acs.nanolett.7b02161.
19. Ji, H.; Ghimire, M.K.; Lee, G.; Yi, H.; Sakong, W.; Gul, H.Z.; Yun, Y.; Jiang, J.; Kim, J.; Joo, M.-K.; et al. Temperature-Dependent Opacity of the Gate Field Inside MoS 2 Field-Effect Transistors. *ACS Appl. Mater. Interfaces* **2019**, *11*, 29022–29028, doi:10.1021/acsami.9b06715.
20. Mead, D.G. Long wavelength study of semiconducting germanium arsenide, GeAs. *Infrared Phys.* **1982**, *22*, 209–213, doi:10.1016/0020-0891(82)90045-8.