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A Tunable CMOS Image Sensor with High Fill-Factor for High Dynamic Range Applications †

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Abstract: Several CMOS imager sensors were proposed to obtain high dynamic range imager (>100 dB). However, as drawback these imagers implement a large number of transistors per pixel resulting in a low fill factor, high power consumption and high complexity CMOS image sensors. In this work, a new operation mode for 3 T CMOS image sensors is presented for high dynamic range (HDR) applications. The operation mode consists at biasing the conventional reset transistor as active load to photodiode generating a reference current. The output voltage achieves steady-state when the photocurrent becomes equal to the reference current similar to the inverter operation in the transition region. At a specific bias voltage, the output swing from o to Vdd in a small light intensity range, however, high dynamic range is achieve using multiple readout at different bias voltage. For high dynamic range operation different values of bias voltage can be applied from each one the signal can be captured and then to compose a high dynamic range image. Compared to other high dynamic range architectures this proposed CMOS image pixel show as advantage high fill-factor (3 T) and lower complexity. Moreover, as the CMOS pixel does not operate in integration mode, de readout can be performed at higher speed. A prototype was fabricated at 3.3 V 0.35 μm CMOS technology. Experimental results as show by applying five different control voltage from 0.65 V to 1.2 V is possible to obtain a dynamic range about 100 dB.

Keywords: CMOS; dynamic range; image sensor; photodetector

1. Introduction

Several image sensor applications, such as in the biomedical, robotics and surveillance areas, require imaging systems with high dynamic range. Typically, imagers for these applications are required to capture scenes with dynamic ranges ~100 dB. However, conventional CMOS image sensors possess dynamic range of only ~60 dB. Therefore, many techniques were proposed to achieve high dynamic range using CMOS image sensors [1–6]. In [2], by integrating a comparator and a dynamic flip-flop in each pixel, a multi-sampling technique, was proposed. In [3], a self-reset technique using one comparator per pixel was described. In general, these techniques are effective as they achieved a dynamic range >100 dB. However, they both require a large number of transistors per pixel, resulting in a low fill factor, high power consumption and high complexity.

More recently, techniques using analog-to-digital converters have been proposed as a method to obtain high dynamic range with high fill-factor and low pixel complexity [7–12]. However these approaches achieves dynamic ranges of 70–80 dB, which is too low for some applications. Therefore,

there is still a need to improve the performance of CMOS active pixel sensors with respect to high dynamic range, high fill-factor and low complexity [13,14].

In this work, we propose a new control method of 3 T CMOS active pixel sensor for high dynamic range applications. It maintains high fill-factor and low complexity compared to main topologies of high dynamic range CMOS image sensors. The main different concept is to keep the reset transistor biased, generating a reference current. The steady-stated of pixel occurs when the photocurrent is equal to charge transistor current. The output voltage varies from 0 to V_{dd} as a quadratic function of the photocurrent generated (light intensity). The prototype was design at 3.3 V 0.35 µm CMOS technology. Measurements results are presented for voltage biased of 0.65 V, 0.74 V, 0.84 V, 1 V and 1.2 V. In general our measurements results shows that for reset transistor operating at moderate inversion (0.65 V, 0.74 V, 0.84 V) the output voltage range is about 1 decade of light intensity. For operation at strong inversion (1 V and 1.2 V) the output voltage range covers 0.5 decades or less. By combining the 5 different measurements it is possible to assemble a 100 dB dynamic range image.

2. Operation Mode

Figure 1 shows the typical 1T pixel architecture. It is composed of a charge transistor (M_1) and a photodiode. A source follower and a select transistor must be also implemented to connect to the output bus, however, for only a pixel analysis purpose they did not were implemented. A external ultra-low bias input buffer were implemented. The charge transistor is biased at a constant voltage ($V_{control}$), establishing a reference current (I_{ref}) that defines the maximum photocurrent measured in the pixel.

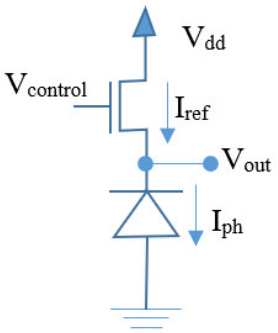

Figure 1. Pixel architecture.

Considering that the operation starts at $V_{out} = 0$ V (see point A—Figure 2) and assuming that the reset transistor's current is higher than the photocurrent, the photodiode´s capacitance voltage (V_{out}) starts to increase due to the difference between the photocurrent and the charge transistor current through the photodiode´s capacitance. As the photodiode's voltage increases, the reset transistor V_{DS} starts to decrease. Being initially in the saturation region (see point A—Figure 2a), the charging transistor's drain current I_{ref} reduces accordingly as V_{DS} reduces. Steady-state is achieved when the photocurrent I_{PH} becomes equals to the charging drain current I_{ref} (see point B in Figure 2).

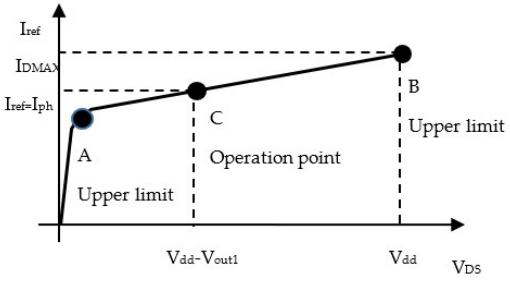

Figure 2. Operation points.

Basically, the output voltage swings from V_{dd} to V_{DSSAT} while the related photocurrent swings from $I_{ref}(V_{dd})$ to $I_{refsat}(V_{DSsat})$. Therefore, the current variation of the reset transistor over the saturation region defines the photocurrent range measured. Considering the typical V-I relationship of MOSFET

$$I_D = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 - \lambda V_{DS}) \quad (1)$$

and knowing that $V_{DS} = V_{OUT} - V_{dd}$ and $I_D = I_{PH}$, Equation (1) can be written as:

$$V_{OUT} = -\frac{L}{W} \frac{1}{\lambda \mu C_{ox} (V_{GS} - V_T)^2} I_{PH} + V_{dd} + \frac{1}{\lambda} \quad (2)$$

Equation (2) shows how the output voltage changes with photocurrent for reset transistor operating at saturation region and $V_{GS} > V_T$.

3. Material and Methods

A light source Spectra Physics with a tungsten halogen lamp illuminates the IC pixel a 550nm filter. A external low bias buffer (femtoamperes) were used to connect the pixel output to a Tektronix oscilloscope. The optical power is varied by changing current lamp. A power meter with calibrated photodetector (Newport) was used to measure the optical power at the same positions as where the chip was placed. For a fixed $V_{control}$ value, the light intensity were increased until the output voltage swing from 0 to V_{dd}.

4. Results and Discussion

A prototype was fabricated at 0.35 μm 3.3 V AMS CMOS technology. The pixel comprise a 10 μm × 10 μm Nwell-Psub photodiode and a W/L = (0.4 μm/0.4 μm) presenting fill-factor about 80%. Figure 3 shows the output voltage of the pixel obtained from measurements at five different control voltages. As one can see, the pixel photoresponse curves at V_{GS} = 1.2 V and V_{GS} = 1.0 V the output voltage range is about 3 V and the dynamic range is very small, less than 20 dB. This biasing condition and photoresponse is characterized by the pixel operating at strong inversion. The pixel photoresponse curves at V_{GS} = 0.84 V, V_{GS} = 0.74 V and V_{GS} = 0.65 V the output voltage range is about 3 V and the dynamic range is small but higher increasing toward 20 dB as V_{GS} reduces.

Although, the photoresponse shows small dynamic range, by using multiples captures from the five control voltages it is possible to achieving 5 decades of photocurrent values or image with a 100 dB dynamic range. Moreover, the new operation mode with small dynamic range allow to see small contrast image parts at conventional pixel into a full N bits image. Therefore the small dynamic tunned photoresponse gives as unique characteristic to offer a image enhanced of small contrast images been very attractive for surveillance and medical cameras applications.

Compared to most linear CMOS active pixels with high dynamic range [1–6], the main advantage of our proposed pixel is to integrate a small number of transistors per pixel, thus achieving higher fill-factor and small pixel complexity. In general, the fill factor of HDR architecture in the literature [1–6] varies from 15% to 50% in while our 4T pixel has a fill-factor of ~80% using a 10 μm × 10 μm photodiode. The main drawback of low fill-factor is the reduction of the global quantum efficiency 15.

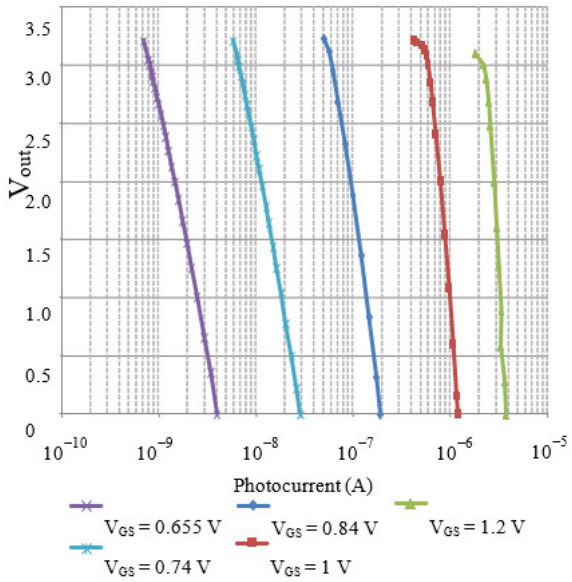

Figure 3. Pixel photoresponse: output voltage versus light intensity at five different control voltages.

3. Conclusions

A new operation mode for 3 T CMOS image sensors prototype fabricated at 0.35 μm 3.3 V AMS CMOS technology for high dynamic range is presented. The pixel output voltage is related to photocurrent and it is controlled (tunned) by a voltage. For operation at only one bias voltage the output shows less 10 decades of dynamic range. This application allow a typical low contrast image portion at full N bits image providing image enhancement. Multiples captures using multiples bias voltages allows to achieve a dynamic range image equal or greater than 100 dB. The fill-factor is about only 80% and it is very higher than typical high dynamic range imager architectures. As overall characteristic, this new control method comprise a conventional 3 T pixel architecture offering simultaneously high dynamic range, high fill-factor, low pixel complexity and wide output swing range. Moreover, for small dynamic range this pixel can be used at tuned image enhanced cameras.

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