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Effects of electrical stress in solution-processed Spin-on Glass dielectric films: Frequency dependence

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Abstract: Currently, the stability of field-effect devices based on emerging technologies is one of the most demanding research issues in terms of performance. Since solution-processed electronic devices are attracting much attention to enable low-cost flexible electronics, the reported studies of stability seem to be conceived with arbitrary conditions. In this work, the effects of the frequency dependence of transparent dielectric based on Spin-on Glass (SOG) under electrical stress is presented. The SOG thin films were cured at 200°C in air ambient. The capacitance-voltage and capacitance-frequency characteristics were measured in Metal-Oxide-Semiconductor (MOS) capacitors using the SOG thin film. In addition, electrical stress is applied to the MOS capacitors at different voltage values and during a long period of time. The results show, depending on the bias stress applied, a reversible interface charge contribution and an irreversible charge induced by interface states probably generated by the degradation of the film.

Keywords: solution-processed; electrical stress; spin-on glass

Introduction

Currently, the stability of field-effect devices based on emerging technologies is one of the most demanding research issues in terms of performance. Since solution-processed electronic devices are attracting much attention to enable low-cost flexible electronics, the reported studies of stability seem to be conceived with arbitrary conditions. Frequently, they do not give explanation for the stress conditions used or the same values of electrical stress previously reported were considered, regardless the gate dielectric thickness and structure of the device.

Moreover, only few studies can be found in literature about this topic in solution-processed dielectric films[1].

[1] A. Kumar et al. Mater. Sci. Semi. Proc. 2015; 40:77-83

Introduction

In this work, the effects of electrical stress in solution-processed dielectric film are presented. In particular, the frequency dependence of transparent dielectric based on Spin-on Glass (SOG) under electrical stress is presented. Electrical stress is applied to MOS capacitors at different voltage values and during a period of time. It is important to note that SOG films have been previously used as gate dielectric in Planarized a-SiGe:H TFTs, flexible zinc nitride TFTs and flexible AZO diodes.

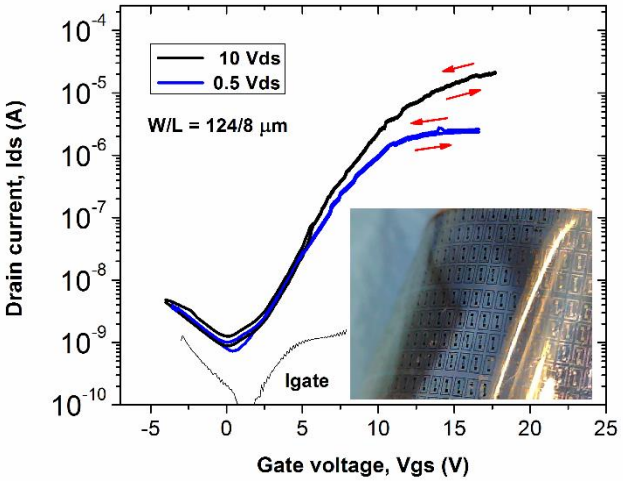

Fig 1. Flexible Zinc Nitride TFTs using SOG [2]

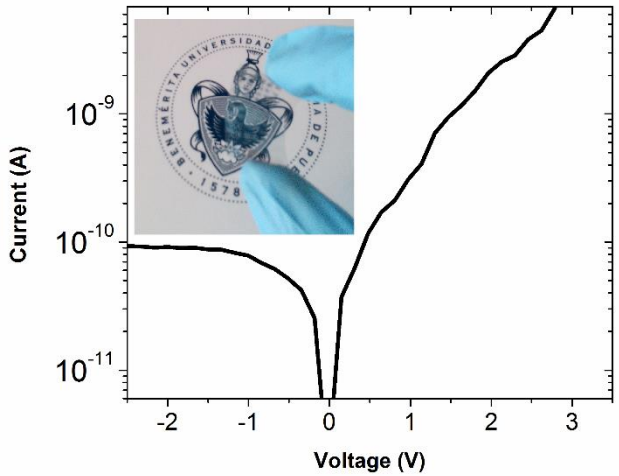

Fig 2. Flexible AZO MIS diodes using SOG [3]

[2] M. Dominguez et al. IEEE Trans. Electron. Dev. 2018; 65(3): 1014-1017
[3] M. Dominguez et al. Thin Solid Films. 2018; 645: 278-281

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Results and Discussion

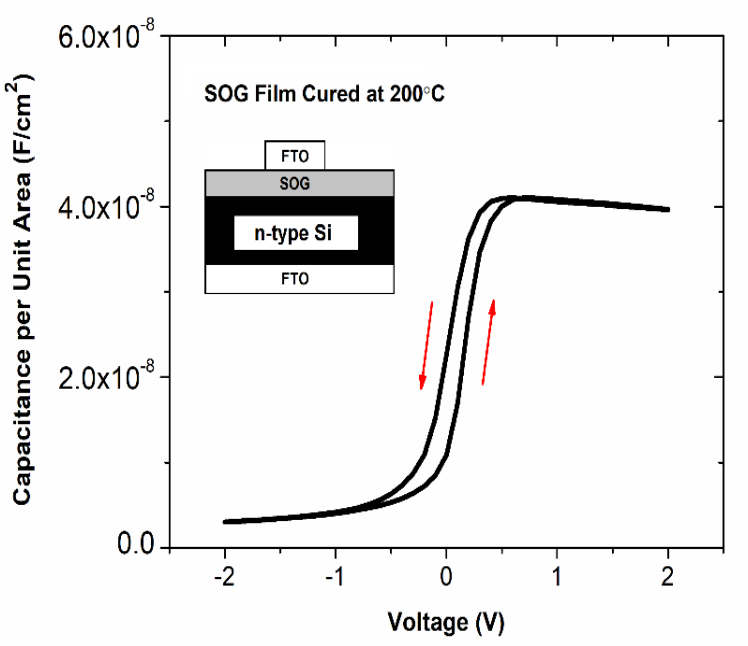

Figure 1. Capacitance-voltage characteristics for the n-type MOS capacitors.

The characteristics show a well-defined accumulation region when a positive voltage is applied at the top contact, as the positive voltage increases there is an accumulation of electrons at the dielectric-semiconductor interface (SOG-Si), increasing the capacitance. When a negative voltage is applied at the top contact, a depletion region is induced, then, the capacitance decreases [4].

[4] D. Neamen, Semiconductor physics and devices. 3ed. Mc. Graw Hill (2003)

Results and Discussion

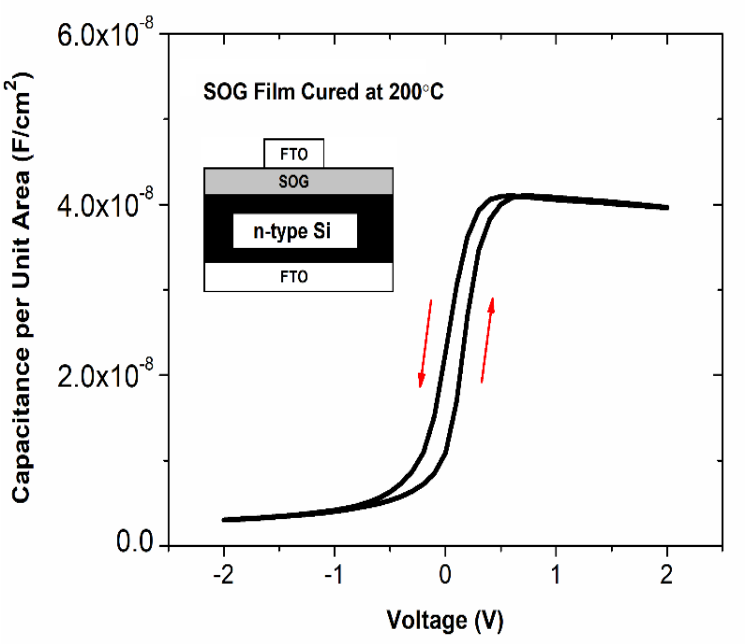

Figure 1. Capacitance-voltage characteristics for the n-type MOS capacitors.

Field-effect devices, such as Thin-film Transistors, work in accumulation where the channel layer is formed at the dielectric-semiconductor interface. Therefore, in order to study the frequency dependence under electrical stress, the capacitance is measured in the accumulation region of the MOS capacitors (2V).

Results and Discussion

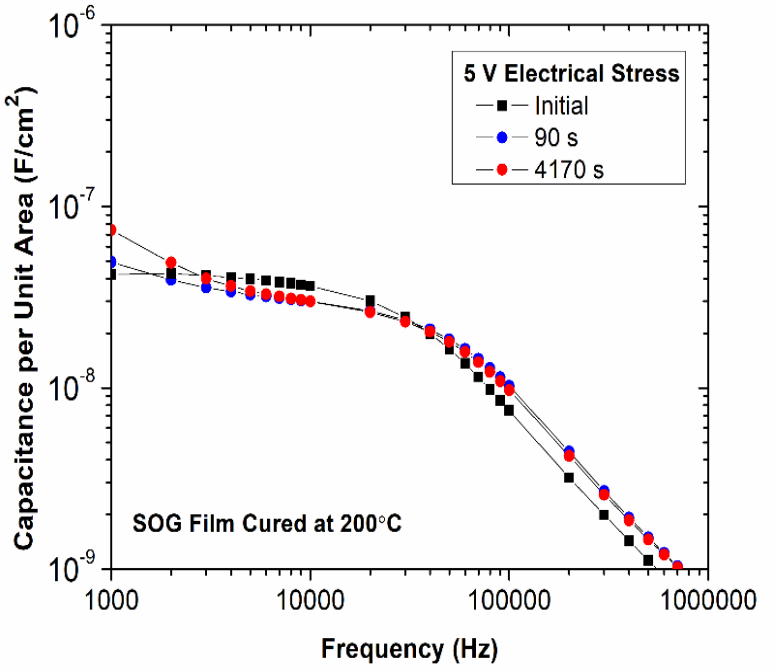

Figure 2. Frequency dependence characteristics for different stress time at 5V electrical stress.

It can be observed a frequency dependence, or also called frequency dispersion, at the initial measurement due to interface states [4].

The electrical stress induce charge trapping at the dielectric-semiconductor interface (interface charge). This interface charge causes variations in the accumulation capacitance. It can be observed, that after a long stress time, the characteristics are very similar.

[4] D. Neamen, Semiconductor physics and devices. 3ed. Mc. Graw Hill (2003)

Results and Discussion

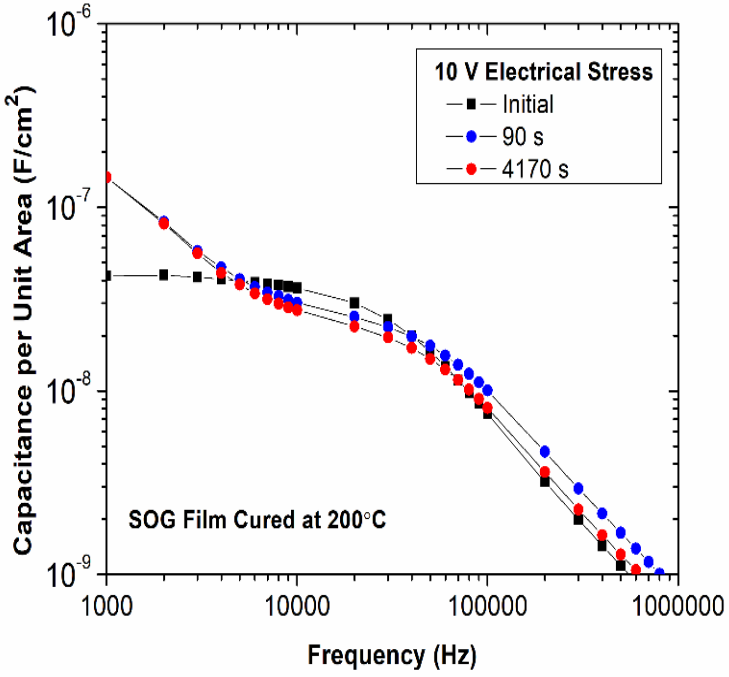

Figure 3. Frequency dependence characteristics for different stress time at 10V electrical stress.

At high frequencies, the accumulation capacitance after electrical stress exhibit similar values than the initial measurement. However, it is clearly exhibited an increase of the accumulation capacitance at 1-4 KHz due to the higher electrical stress.

This behavior can be due to residuals during the deposition of the films. Since our SOG dielectric films are deposited at low temperature, probably some residuals interact with the electrical stress, inducing additional charges. These induced charges can follow the low frequency contributing to the accumulation capacitance [5].

[5] S. Kaya et al. J. Alloy Compnd. 2014; 583:476-480

Results and Discussion

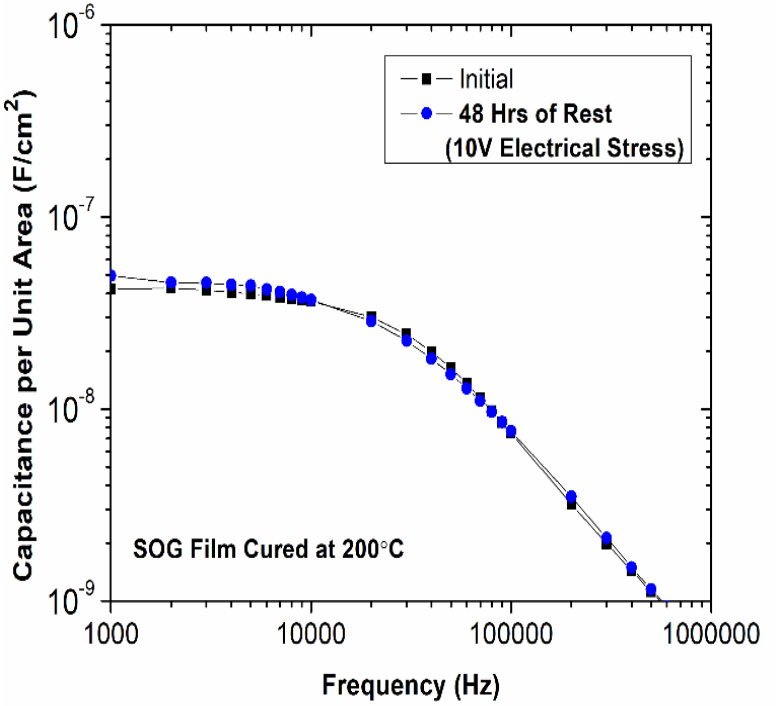

Figure 4. Comparison of the initial and 48 Hrs. rested capacitance-frequency characteristics after 10V electrical stress.

The MOS capacitors were kept in rest for 48Hrs and measured again.

The characteristics were reestablished, indicating that **most of the interface charge is reversible** as many authors suggest [6,7].

[6] M. Powell et al. Appl. Phys. Lett. 1987; 51:1242-1244
[7] F. John and J. Conley. IEEE Trans. Dev. Mater. Reliab. 2010; 10:460–474

Results and Discussion

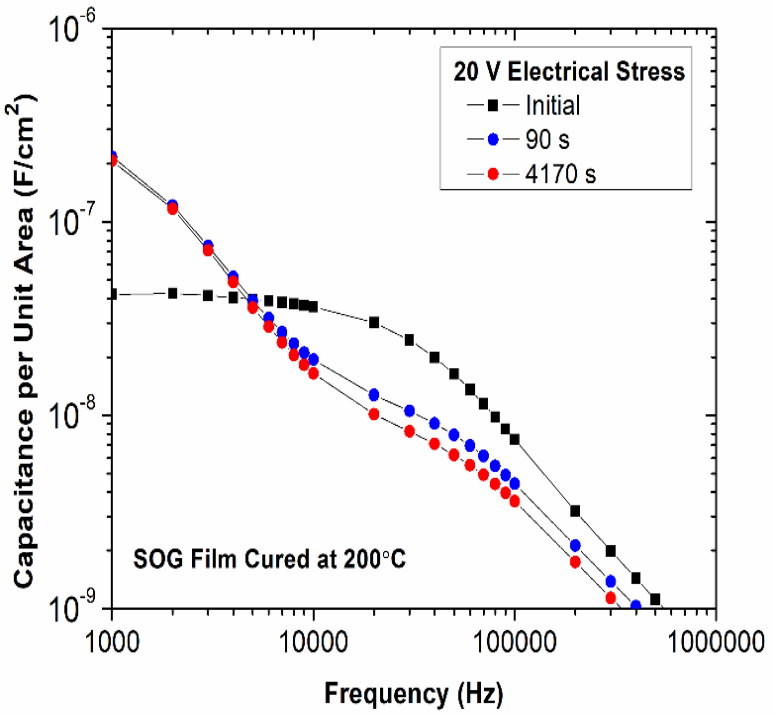

Figure 5. Frequency dependence characteristics for different stress time at 20V electrical stress.

A higher electrical stress was induced by applying 20V for different times.

There is a decrease in the accumulation capacitance that can be related to a reduction of the accumulation charge in the MOS capacitor, probably by tunneling of electrons through the dielectric [8].

Also, the accumulation capacitance at 1-4 KHz is increased by the additional interface states.

[8] D. Schroder, Semiconductor material and device characterization, Wiley, New York (1998)

Results and Discussion

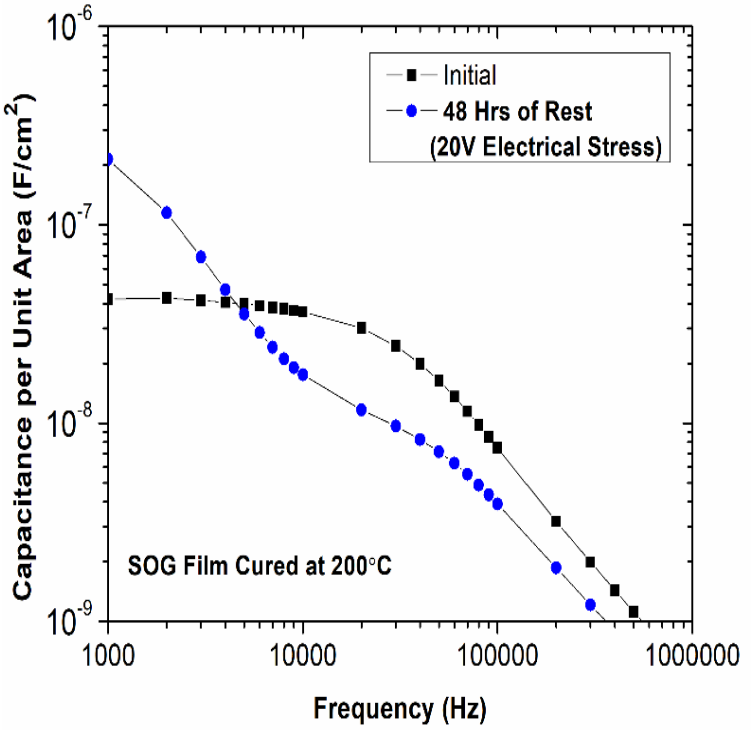

Figure 6. Comparison of the initial and 48 Hrs. rested capacitance-frequency characteristics after 20V electrical stress.

The MOS capacitors were kept in rest for 48Hrs and measured again.

It is appreciated that the characteristics are irreversible after 48Hrs of rest. This suggests that the higher electrical stress induce **an irreversible degradation** in the dielectric film by a higher tunneling rate through the dielectric, where these carriers slowly degrade the dielectric film making irreversible the effects of the electrical stress [9].

[9] M. Dominguez et al. J. Alloy Compnd. 2016; 688: 893-896

Conclusions

The low electrical stress induce charge trapping at the dielectric-semiconductor interface (interface charge) which causes variations in the accumulation capacitance.

The variations at low electrical stress in capacitance are reversible after a period of rest.

The results suggest that high electrical stress induce a degradation of the film, resulted by the probable interaction of the residuals within the film with the electrical stress. This behavior is irreversible.

This work presents a study to find an optimum range of stability in dielectric films under electrical stress.

Acknowledgments

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